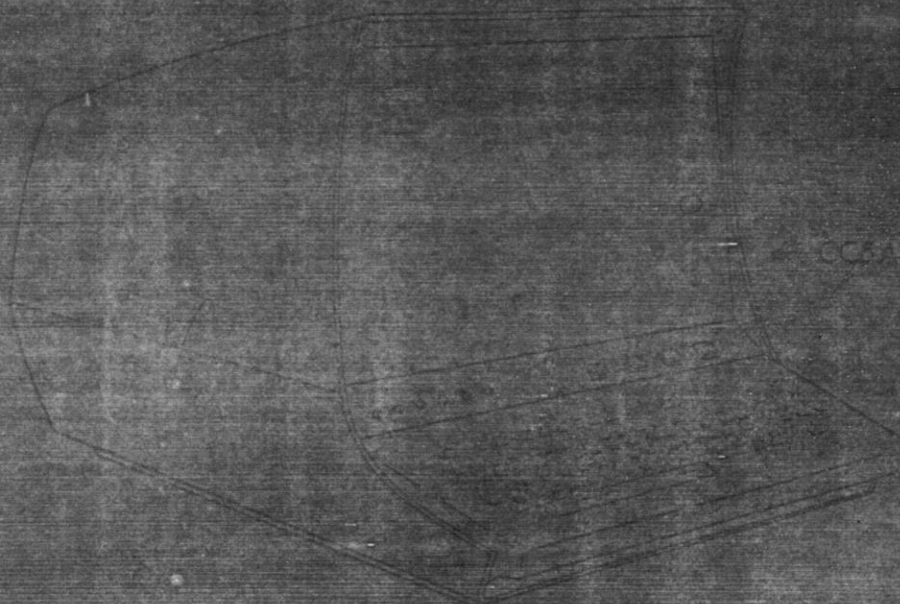


CONTROL DATA

GEM 92413 20 CONVERSATIONAL DISPLAY TERMINAL

INTRODUCTION

THIS MANUAL IS INTENDED FOR THOSE
PERSONS WHO ARE RESPONSIBLE FOR
THE INSTALLATION, OPERATION, AND
MAINTENANCE OF THE GEM 92413 20
CONVERSATIONAL DISPLAY TERMINAL.



GEM 92413 20 Display/Keyboard



ON-SITE MAINTENANCE MANUAL

OEM 92413-20

CONVERSATIONAL DISPLAY TERMINAL
ON-SITE MAINTENANCE MANUAL

SECTIONS IN THIS MANUAL:

- Section I — General Description
- Section II — Operation
- Section III — Installation and Checkout
- Section IV — Preventive Maintenance
- Section V — Fault Isolation
- Section VI — Corrective Maintenance
- Section VII — Spare Parts Catalog

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St. Paul, Minnesota 55113

OEM 92413-20
CONVERSATIONAL DISPLAY TERMINAL
ON-SITE MAINTENANCE MANUAL

[illegible]

AA 4223

CONFIGURATION INFORMATION

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that FCO number and all of the FCO numbers underneath it match all of the FCO numbers on the equipment FCO log, then this manual accurately reflects the equipment.

Equipment Type	Series	With FCO's	Equipment Type	Series	With FCO's
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FOREWORD

This publication serves as an On-Site Maintenance Manual for servicing the OEM 92413-20 Conversational Display Terminal. Basically this terminal is the 208/230 volt, 50 Hz type defined as equipment and may include the following options:

<u>PRODUCT</u>	<u>NAME</u>	<u>EQUIPMENT</u>
OEM 68277	Expanded Memory Kit	CC311-A (Internal)
OEM 92427	Non-Impact Printer, 50 Hz	CN503-B (External)

Expanded Memory optional equipment is described in this manual.

A separate manual (OEM 92427 Receive-Only Non-Impact Printer Station, On-Site Maintenance Manual) applies for the optional external printer.

The terminal acts as a remote message I/O station operating primarily within a central processor controlled telecommunications system. The terminal provides standard teletypewriter I/O functions and as such may serve as a replacement for teletypewriter remote terminals. An output channel is contained in the terminal to enable use of an optional printer to obtain hardcopy of displayed messages.

Information supplied in this manual is limited to that which will aid maintenance personnel in carrying out the plan of on-site removal and replacement of modular units rather than isolation of a fault to a discreet part. This approach, and the simplicity of the modular equipment design allows effective equipment maintenance and, at the same time, minimizes the problem of knowledge retention that occurs when an individual is responsible for a large number of varied equipments.

This manual consists of seven sections. General Description defines the Conversational Display Terminal. Operation describes controls and operating procedures. Installation and Checkout is self explanatory. Preventive Maintenance describes several housecleaning tasks — there are no operational procedures required. Fault Isolation provides procedures and fault symptoms to guide troubleshooting. Corrective Maintenance contains remove and replace procedures and adjustment procedures required to correct faults. Spare Parts Catalog contains genealogy charts, spare parts lists, and assembly diagrams to aid on-site assembly/parts replacements.

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SECTION I

GENERAL DESCRIPTION

This section defines the Conversational Display Terminal (Figure 1-1), and typical applications. This equipment replaces teletypewriter remote terminals on either leased or dial telephone lines with a fast, quiet, video telecommunications terminal which provides an operator with composition versatility not possible with a conventional teletypewriter terminal. The terminal is designed for teletypewriter communications system compatibility and is ready for immediate use with CCITT V 24 interface data sets (modems) which operate in asynchronous mode up to 300 Baud data transfer rate. This interface is compatible with EIA Standard RS-232-C and the modem required is equivalent to the AT&T 103 Series.

FEATURES.

The terminal contains the following important features:

- Standard teletypewriter keyboard layout with simplified Tri-level operation and additional convenience controls.
- Quiet, reliable magnetic-reed-switch keyboard.
- 96 USASCII * alphanumerics (characters)
- 32 USASCII * control codes
- Scroll and page format.
- Non-destructive blinking cursor (dash underline).
- Cursor control for up, down, left, right, and home.
- Inverse video (black on white) where desired.
- Display character size 1/4 inch high by 1/8 inch wide (nominal) formed by 5 x 9 dot matrix using a standard 262-line television raster.
- 8 lines of 80 characters. (640 characters) with built-in expansion capability to 16 lines of 80 characters (see "Optional Features").
- 50 Hz display refresh rate.
- Metal oxide semi-conductor memory (MOS).

*USA Standard Code for Information Interchange per American National Standards Institute X3.4 - 1968.

CCITT V 24 interface (RS-232-C compatible) capable of asynchronous, serial, data transmission at 75, 110, 150, 200, and 300 Baud.

Switch selections for: Full or Half duplex; Odd, Even, or no parity; Keyboard lockout; Remote or Local; Scroll or Page format; selectable Baud Rate, Printer on/off line.

Output channel for optional hardcopy printer.

Modular construction for quick field repair.

OPTIONAL FEATURES.

Modular display character memory expansion of additional 640 characters--easy field installation. This provides a display of 16 lines of 80 characters.

Receive-only hardcopy printer. This separate equipment may be plugged to the terminal to provide permanent copy of messages sent or received.

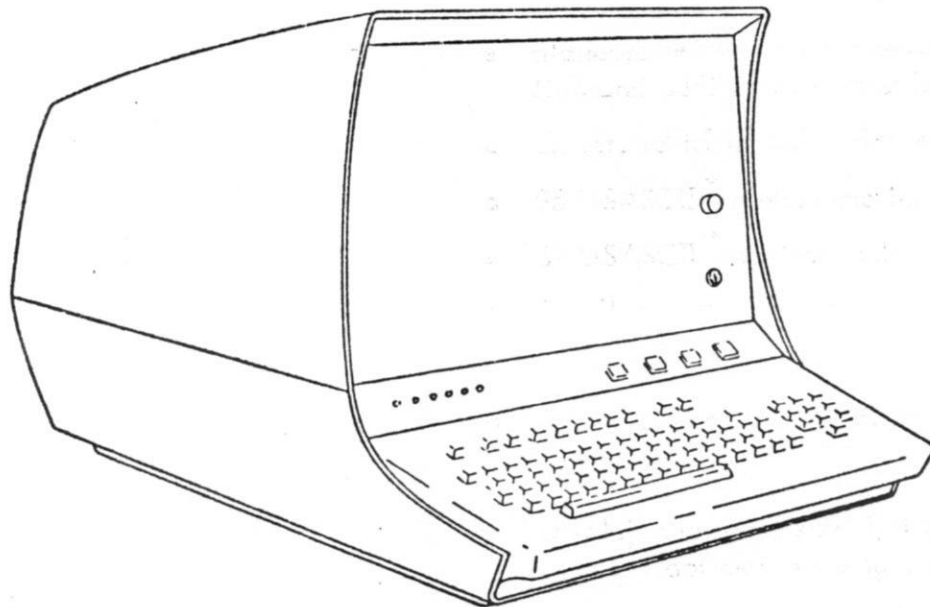


Figure 1-1. Conversational Display Terminal

TYPICAL SYSTEM APPLICATION.

The terminal will operate as a remote terminal in communications systems which provide CCITT V 24 modem interface for two-way communication. With this type interface provided, the terminal will operate in a time-sharing, central processor controlled, communications system as shown in Figure 1-2. Communications are performed in a serial character-by-character fashion without "block" transfers.

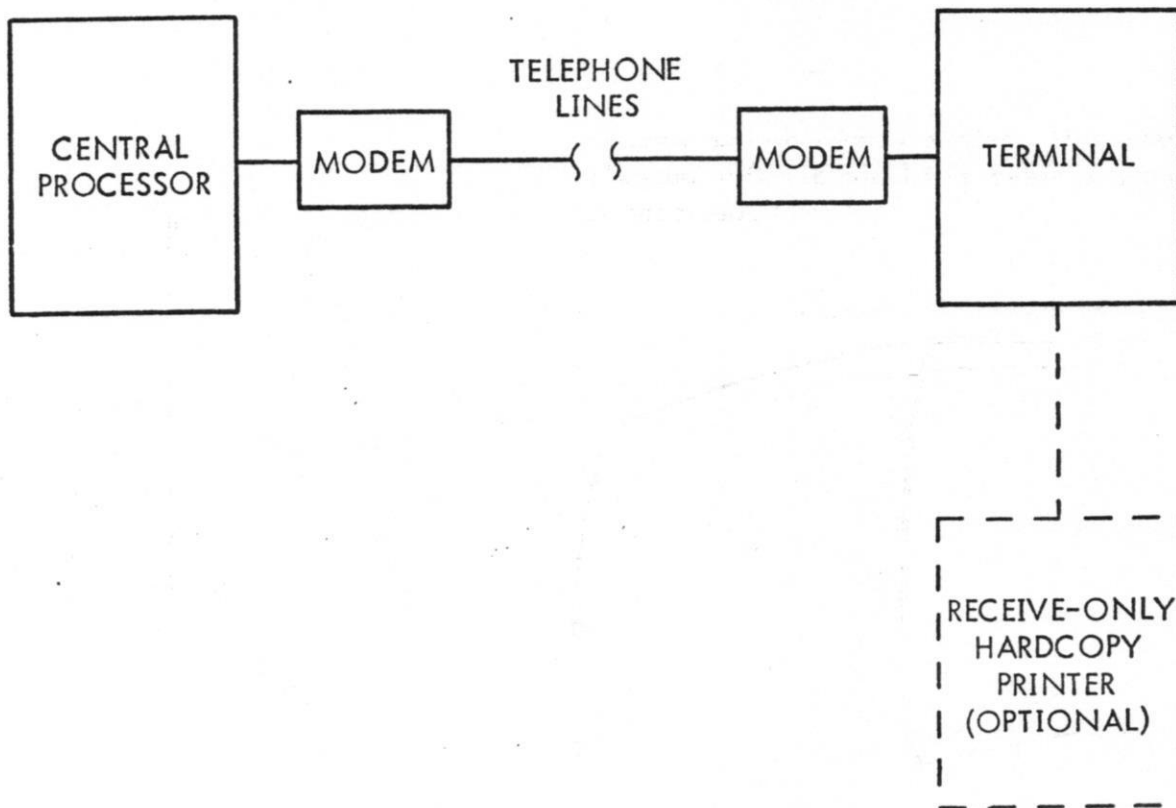


Figure 1-2. Communications Application of Basic Terminal

ELECTRICAL AND PHYSICAL CHARACTERISTICS.

POWER REQUIREMENTS

Equipment CC5A4-B: 208/230 volts, 50Hz, 0.75A Max.

ENVIRONMENT

Operating Temperature: 10°C to 35°C (50°F to 95°F).

Storage Temperature: -10°C to +50°C (+14°F to +122°F).

Operating Humidity: 20% to 80% - no condensation.

Storage Humidity: 10% to 90% - no condensation.

Operating Altitude: -305 met. to 2745 met. (-1000 ft. to + 9,000 ft.)

Storage Altitude: -305 met. to 4572 met. (-1000 ft. to + 15,000 ft.)

HEAT DISSIPATION

700 Btu/hr.

DIMENSIONS

Height: 46 cm. (18 in.)

Width: 46 cm. (18 in.)

Depth: 74 cm. (29 in.)

Weight: 34 ka. (75 lb.)

SECTION II

OPERATION

This section contains a basic operational description of the terminal and is intended to acquaint the reader with the functional and manual operations of the equipment. Topics covered are: functional operation (internal and interface), operator controls and indicators, maintenance controls and indicators, applying power, data entry, and options.

FUNCTIONAL OPERATION.

The terminal contains seven basic functional areas (see block diagram in Figure 2-1) located within four modular subassemblies as shown in Figure 2-2.

- 1) TV display module with associated drive circuits.
- 2) Modular, 640 character read/write memory.
- 3) Control logic.
- 4) Data entry keyboard.
- 5) Asynchronous modem interface.
- 6) Serial output channel for an optional hardcopy printer.
- 7) Internal power supply.

TV DISPLAY MODULE.

The display portion of the terminal consists of a field replaceable, high resolution, television display module which accepts composite video from the character memory and associated control logic. The basic machine displays 8 lines of 80 characters on a 15-inch (38 cm) diagonal, rectangular CRT within a view screen area approximately 8-inches (20 cm) high by 10-inches (25 cm) wide. An expanded character memory option (see "Options", this section) provides 16 lines of 80 characters. Display repertoire is the USASCII X3.4-1968 compatible set of 96 characters plus three characters generated from function codes (see Table 2-1). Characters appearing on the display screen are dot formed by selectively unblanking positions

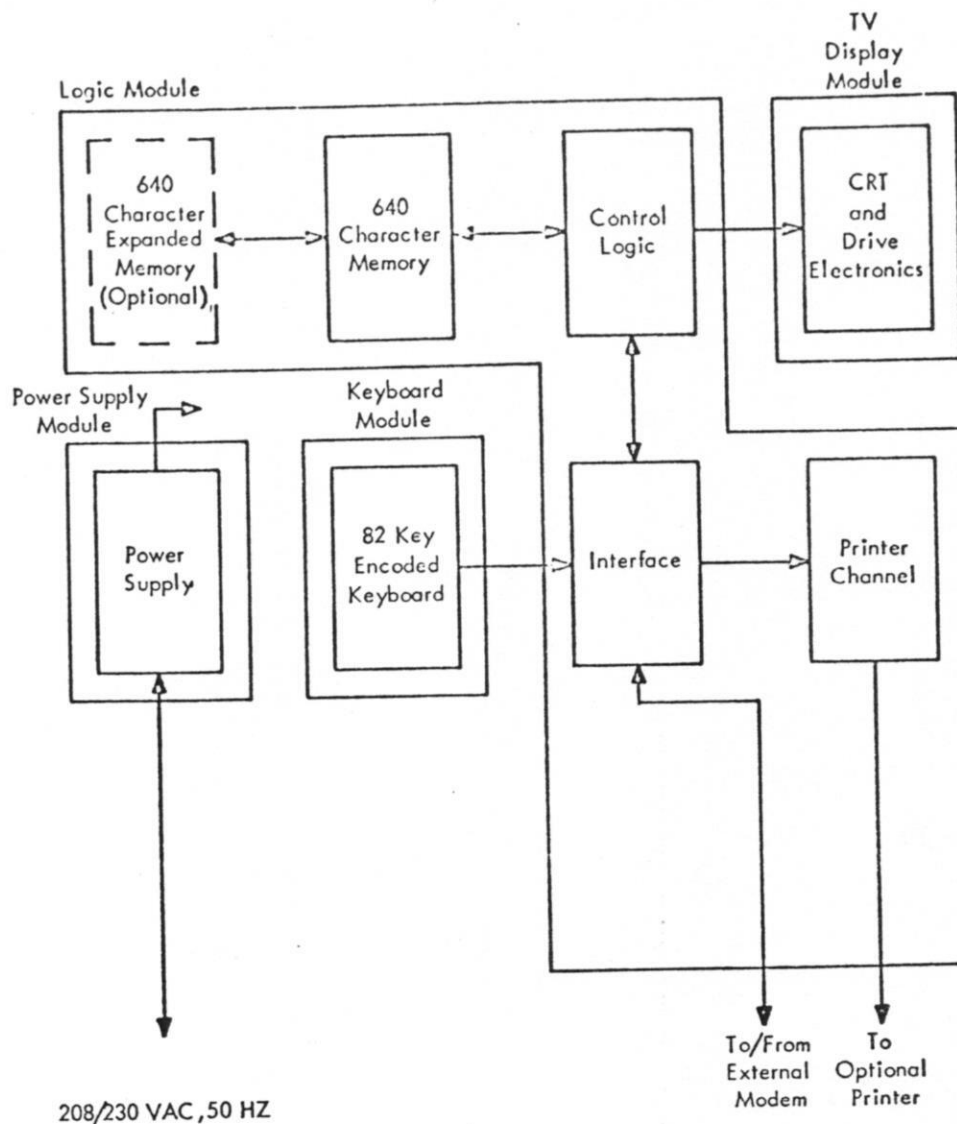


Figure 2-1. Terminal Functional Block Diagram

within a 5 x 9 dot matrix—during a normal television raster scan of 262 horizontal lines. Nominally, the characters appear on the display 1/8 inch (0.3 cm) wide and 1/4 inch (0.6 cm) high. A cursor (entry marker) appears on the display screen as a blinking underline dash to indicate the position where a character will display on the screen. A full display of 8 or 16 lines of 80 characters occupies approximately a 5 inch (13 cm) high and 9 inch (23 cm) wide area of the viewing screen. The display refresh rate is 50 Hz.

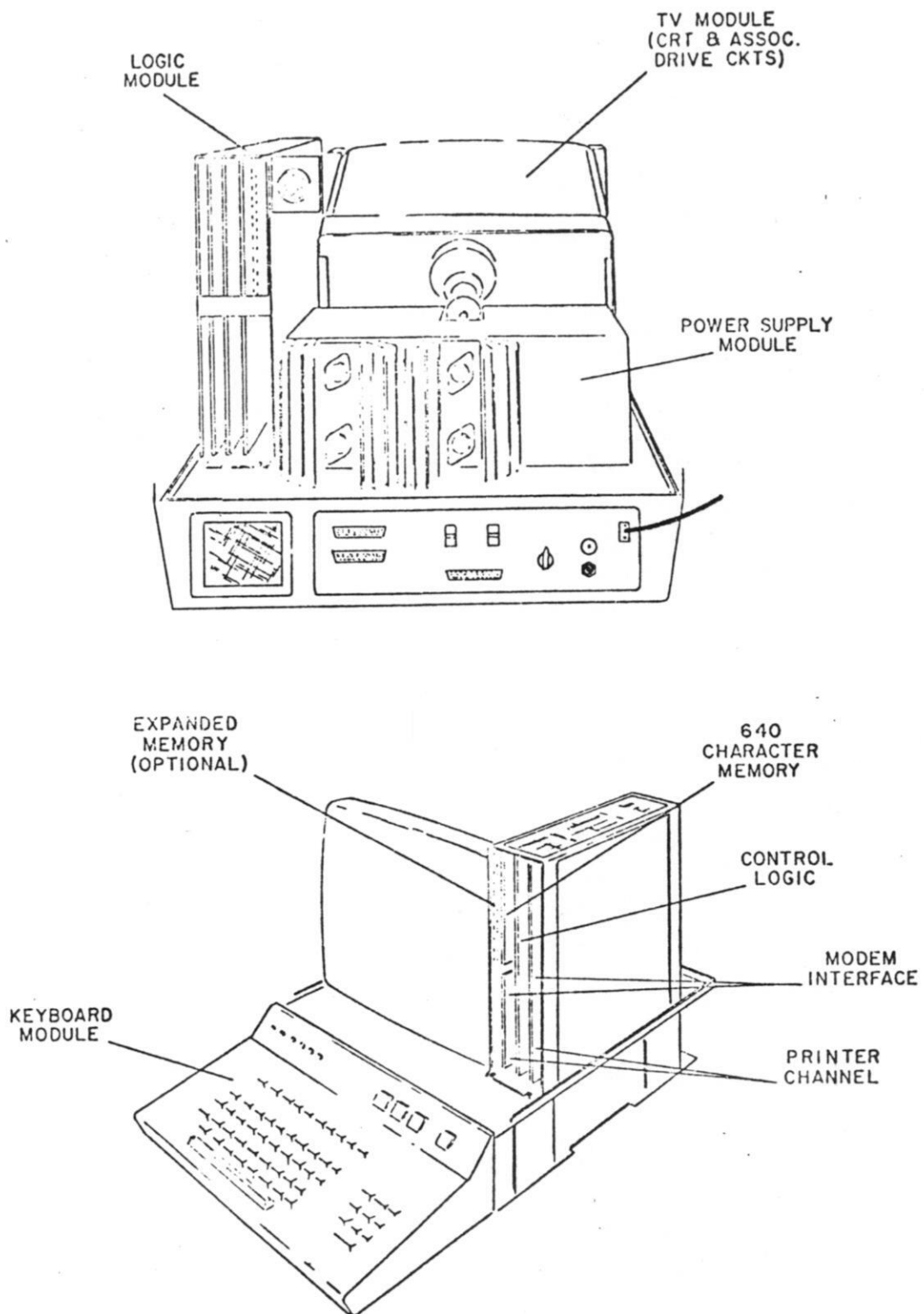


Figure 2-2. Module and Function Locations

TABLE 2-1. DISPLAYABLE CHARACTER REPERTOIRE

OCTAL CODE	CHARACTER	OCTAL CODE	CHARACTER
040	(Space	120	P
041	! (exclamation point)	121	Q
042	" (quotation mark)	122	R
043	# (number or pounds)	123	S
044	\$ (dollar sign)	124	T
045	% (percent)	125	U
046	& (ampersand)	126	V
047	' (apostrophe)	127	W
050	((left parentheses)	130	X
051	) (right parentheses)	131	Y
052	* (asterisk)	132	Z
053	+ (plus)	133	[(left bracket)
054	, (comma)	134	\ (reverse slant)
055	- (hyphen or minus)	135	] (right bracket)
056	. (period)	136	^ (circumflex)
057	/ (slant)	137	_ (underline)
060	0	140	` (left single quote mark)
061	1	141	a
062	2	142	b
063	3	143	c
064	4	144	d
065	5	145	e
066	6	146	f
067	7	147	g
070	8	150	h
071	9	151	i
072	: (colon)	152	j
073	; (semicolon)	153	k
074	< (less than)	154	l
075	= (equals)	155	m
076	> (greater than)	156	n
077	? (question mark)	157	o
100	@ (commercial at)	160	p
101	A	161	q
102	B	162	r
103	C	163	s
104	D	164	t
105	E	165	u
106	F	166	v
107	G	167	w
110	H	170	x
111	I	171	y
112	J	172	z
113	K	173	{ (left brace)
114	L	174	(vertical line)
115	M	175	} (right brace)
116	N	176	~ (equivalent or similar)
117	O	177	␣ (or parity error)
			FUNCTIONS
		003	▲ (ETX)
		016	◀ (Begin Inverse)
		017	▶ (End Inverse)

640 CHARACTER MEMORY.

A modular metal oxide semiconductor (MOS) memory stores 640, 7-bit character codes for display refresh and input/output storage. The memory is contained on one printed circuit card within the on-site replaceable logic module. An additional 640 character expanded memory option is available as a second plug-in card (see Options, this section).

CONTROL LOGIC.

Controlling the internal functions of the terminal is the control logic that, in addition to timing and sequencing circuits, includes a 256 word, 10-bit, MOS read only memory (ROM) which is programmed with the necessary beam blank/unblank dot patterns for video formation of all displayable characters on the display screen. The control logic is contained on one printed circuit card within the on-site replaceable logic module.

KEYBOARD.

The on-site replaceable keyboard module is the operator input device for the terminal. The keys are the magnetic reed type and when depressed generate the USASCII X3.4-1968 compatible codes for the 96 characters which are displayable and 32 control codes (3 of which cause a displayed character). Tables 2-1 and 2-2 show the characters and functions available from the keyboard. Upon key depression, the corresponding character is displayed and/or its code transmitted via the interface circuits to the modem depending on the LOCAL and FULL/HALF Duplex interface mode switch settings (see Operator Controls and Indicators, this section).

MODEM INTERFACE.

The asynchronous modem interface circuits control communication between the terminal and the associated modem. This interface is designed to operate with CCITT V 24 interface. This is compatible to EIA Standard RS-232-C such as with the AT&T 103 Series modem (or equivalent).

Modem Interface Control.

The modem interface control circuits are contained on two printed circuit cards within the on-site replaceable logic module. The interface communicates

TABLE 2-2. CONTROL FUNCTION REPERTOIRE

Mnemonic	Octal Code	Keyboard Operation		Mnemonic	Octal Code	Keyboard Operation	
		CTRL + Key	Separate Key			CTRL + Key	Separate Key
NUL	000	CTRL + @		DLE	020	CTRL + P	
SOH	001		A	DC1	021		Q
STX	002		B	DC2	022		R
• ETX	003		C	DC3	023		S
EOT	004		D	DC4	024		T
ENQ	005		E	• Skip	025		U
ACK	006		F	• Line Clear	026		V
BELL	007		G	EBT	027		W
• BS	010		H	• Clear	030		X
HT	011		I	• Reset	031		Y
• LF	012		J	• Cursor Up	032		Z
VT	013		K	ESC	033		[
FF	014		L	FS	034		\
• CR	015		M	GS	035		]
• SO	016		N	RS	036		^
• SI	017	CTRL + O		US	037	CTRL + -	
			STX				→
			ETX				LINE CLEAR
							CLEAR
							RESET
							↑
							ESCAPE
							FS
							GS
							RS
							US

- Causes the assigned display operation when entered from separate key (except SO & SI which always must be entered by CTRL + key). Causes the assigned display operation when received from a remote device (receive includes echoed data when operating in FULL DUPLEX mode). All other control codes are ignored by the terminal when received, except BELL which causes a sonic alert tone.

at manually adjustable transmission rates of 75, 110, 150, 200, and 300 bits-per-second (Baud). The interface circuits perform all serial-to-parallel and parallel-to-serial conversion, modem control, and during transmission executes the data clocking function.

Modem Interface Signals.

Figure 2-3 shows the signals required for communication between the modem interface connector located on the back panel of the basic terminal and an CCITT V 24 compatible modem. The maximum cable length allowable for any of these signals is 50 feet (15 meters). The following paragraphs define these signals and their operable voltage levels.

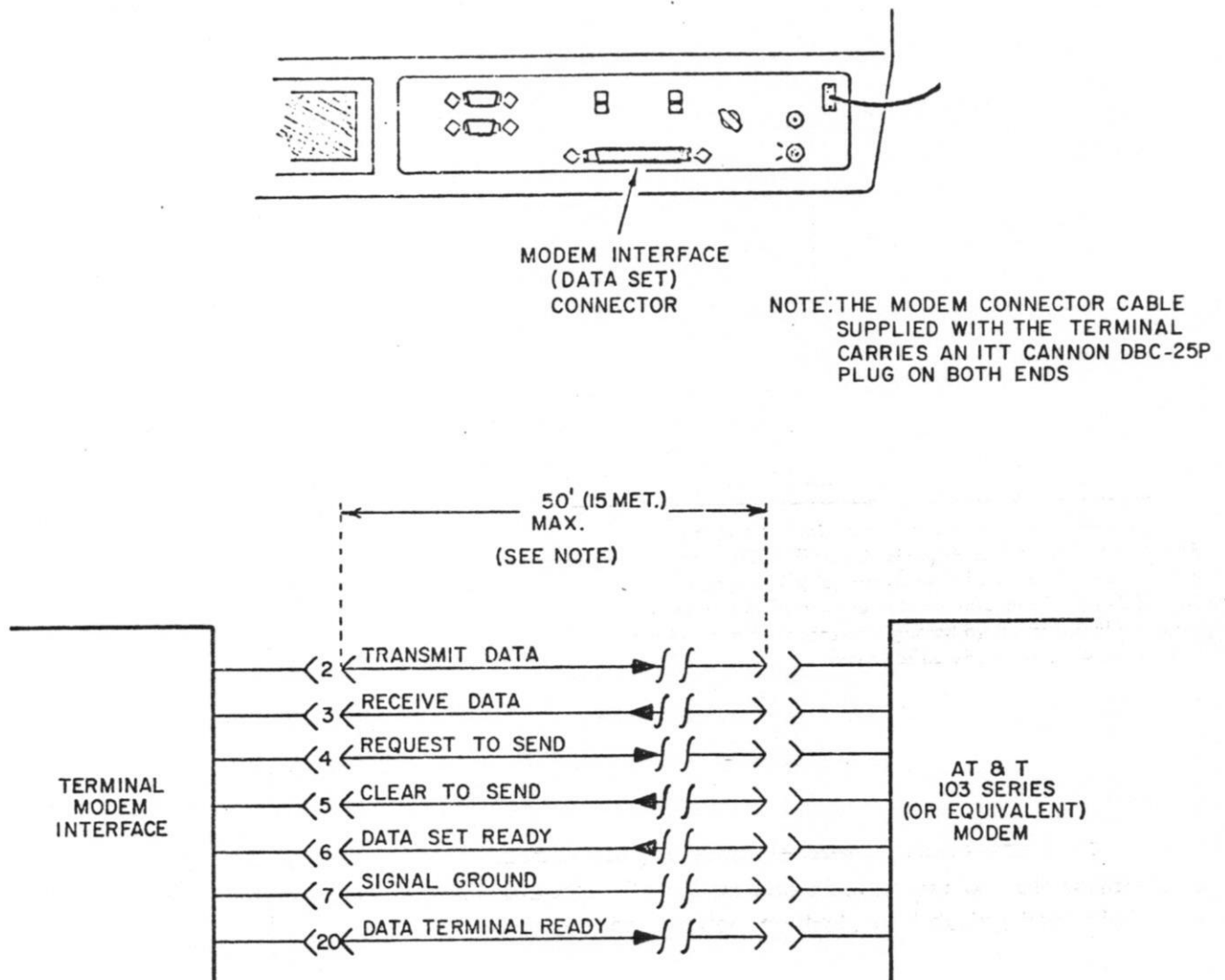


Figure 2-3. Basic Terminal Connector Panel and Modem Interface Signals

Transmit Data.

Data travels from the terminal interface circuits to the modem via the Transmit Data line. When the interface is not transmitting data, the terminal holds the Transmit Data line to a logical 1 (more negative than -3 volts).

Receive Data.

Data travels from the modem to the terminal interface circuits via the Receive Data line. When the modem is not transferring data to the terminal, the modem holds the Receive Data line to a logical 1 (more negative than -3 volts).

Request to Send.

The terminal interface circuits hold the Request to Send line at a logical 0 (more positive than +3 volts) to initiate a transmit operation. The logical 1 state (more negative than -3 volts) on the Request to Send line signifies that the terminal interface circuits are in a receive mode.

Clear to Send.

The modem sets the Clear to Send line to a logical 0 (more positive than +3 volts) in response to the Request to Send signal from the terminal interface circuits. The Clear to Send line becomes a logical 0 within 8 to 210 milliseconds after the Request to Send signal is made positive (active) by the interface. Time variation occurs because of turn-around time of the common carrier. The Clear to Send line remains active until the interface drops the Request to Send line to negative (inactive). At this time, the modem drops the Clear to Send line (inactive) and the terminal interface circuits return to a receive communications mode.

Data Set Ready.

The modem makes this signal line active (more positive than +3 volts) when the modem is in the data mode. This means that the modem is not in the idle or talk mode, nor is it without power.

Signal Ground.

This signal is the voltage base from which the control and data signal voltage levels are referenced. This ground level is connected to protective ground and a-c power ground in the display portion of the terminal.

Data Terminal Ready.

This signal becomes active (more positive than +3 volts) when power is applied to the Conversational Display Terminal if the Continuous DTR strap option is in place and becomes active only when the terminal is in Remote operating mode if the Local DTR strap option is used. See "Strap Options", this section.

PRINTER CHANNEL.

The terminal is designed with a serial printer output channel accompanying the modem interface on the two interface cards contained in the logic module. This channel will accommodate a low-speed hardcopy printer which the customer may obtain to complement the basic terminal.

Printer Channel Control.

Either full-screen (page) printout or instantaneous printout of data when displayed character-by-character, is available by the printer controls included in the basic terminal (see Operator Controls and Indicators, this section). The printer channel presents data to a printer on a 7-bit USASCII character word basis, bit-by-bit serially. All character codes 040₈ through 176₈ shown in Table 2-1 and the control codes for Backspace (010₈), Line Feed (012₈), and Carriage Return (015₈) are intended for a printer. The channel circuits contain "printer-in-use" recognition and drive circuits which allow up to eight terminals to share one low-speed printer.

Presence of a printer does not affect operation of the basic (8 line x 80 character) terminal or the expanded line option (16 line x 80 character) configuration as described in the preceeding portion of this manual, except that during a print operation, the keyboard is disabled and the printer channel I/O signals are used by the terminal interface and control circuits to sequence displayable data codes to the printer.

Printer Channel I/O Signals.

Two printer interface connectors are located at the rear of the terminal on the connector panel. These two connectors are wired internally in a daisy chain fashion with Pin 1 of J1 connected to Pin 1 of J2, Pin 2 of J1 connected to Pin 2, etc. (see Figure 2-4). This allows the terminal to be connected with as many as seven other terminals and a single printer (see Figure 2-5). The total cable length that can be used in any printer application is 1500 feet maximum. Figure 2-4 identifies the required printer interface signals. The communication technique is bi-directional, differential, long-line driver/receiver combination thus each interface signal requires a negative (-) and a positive (+) line as a twisted pair as shown in Figure 2-4. The following paragraphs describe printer interface line functions.

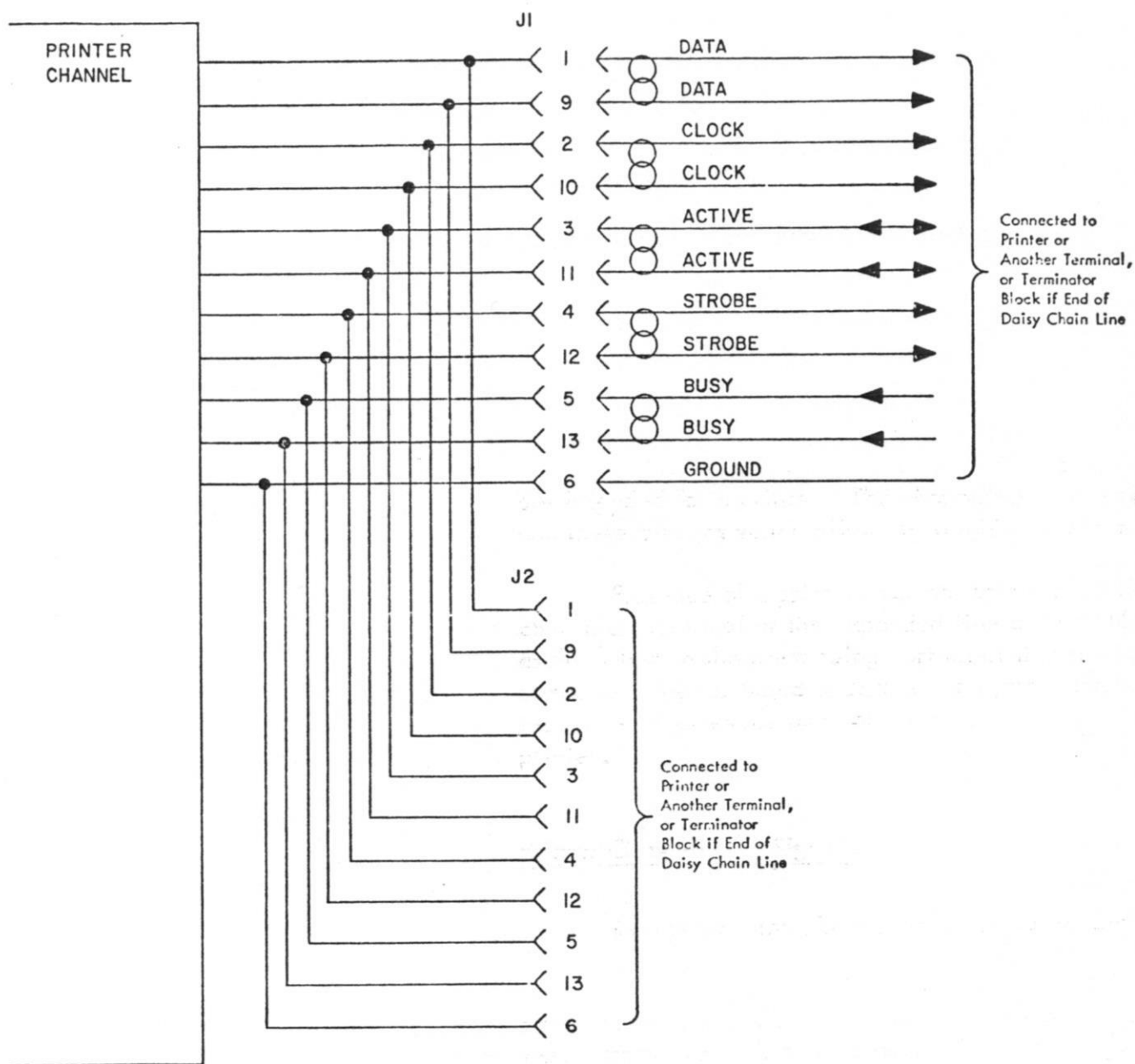
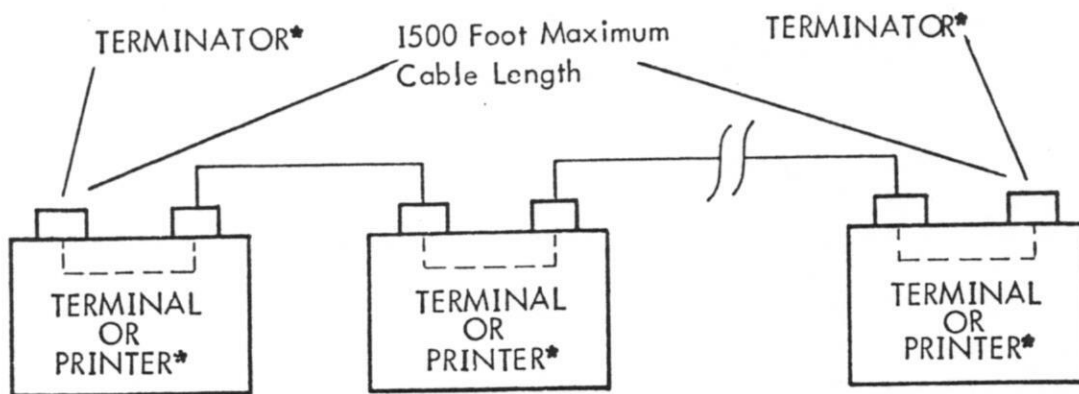


Figure 2-4. Printer Channel I/O Signals



*From one to eight terminals may share one printer. Printer may be located between terminals on the interface line or on either end. Terminator blocks must be installed on the spare connector of the device (terminal or printer) located on each end of the interface.

Figure 2-5. Terminal/Printer Interface

Data.

Changing states of the positive (+) and negative (-) line pair signify binary bits of the USASCII X3.4-1968 compatible codes used for data transmission to the printer.

Data Bit "1" Condition	Pin 1 + current sinking
	Pin 9 - open
Data Bit "0" Condition	Pin 1 + open
	Pin 9 - current sinking

Clock.

The terminal issues a clock signal via the clock line pair whenever it has a data bit condition established on the data line pair and sufficient time has elapsed for the signal to stabilize. The clock signal commands the printer to sample the data line pair for a valid data bit.

Clock (Logic "1" condition)	Pin 2 + current sinking
	Pin 10 - open
Not Clock (Logic "0" condition) . . .	Pin 2 + open
	Pin 10 - current sinking

Active.

The active line pair indicates that one of the terminals connected to the printer is using the printer. Whichever terminal is placed in use with the printer, that terminal's active line driver places the active line in a "being used" condition so that any other terminals connected to the printer recognize that it is in use and not accessible by them.

Active (Logic "1" condition)		Pin 3 + current sinking
		Pin 11 - open
Not Active (Logic "0" condition)	..	Pin 3 + open
		Pin 11 - current sinking

Strobe.

The terminal issues a strobe signal via the strobe line pair whenever it has completed sending all seven data bits of USASCII code to the printer via the data line and clock signal operations. The strobe signal commands the printer to translate and execute the complete data word it has just received.

Strobe (Logic "1" condition)		Pin 4 + current sinking
		Pin 12 - open
Not Strobe (Logic "0" condition)	..	Pin 4 + open
		Pin 12 - current sinking

Busy.

The printer uses the busy line pair to indicate to all terminals connected to it that it is internally busy (during print head return, etc.) and cannot receive data.

Busy (Logic "1" condition)		Pin 5 - open
		Pin 13 + current sinking
Not Busy (Logic "0" condition)	...	Pin 5 - current sinking
		Pin 13 + open

Ground.

The ground signal line establishes a common reference ground for signal levels between Terminals and the printer. Pin 6 carries the ground.

POWER SUPPLY.

The power supply is a solid-state, full-wave transformer type. The power supply module uses 208/230 volt, 50 Hz primary power to supply internal required power of +5 VDC, - 12 VDC, +12 VDC, +73 VDC, and 6.3 VAC. The control logic and keyboard use +5 VDC. The keyboard also uses - 12 VAC. The +12 VDC drives the character refresh memory. +73 VDC drives the TV module circuits. 6.3 VAC supplies current to the CRT heater element. The power supply is an on-site replaceable module and should normally be returned to a repair depot for any necessary adjustments.

The power supply is linear-regulated with foldback current limiting. A transformer, rectifiers, and capacitive filters supply the d-c input for each of the regulators for the four d-c voltages. A separate integrated-circuit regulator controls the current flow of a series pass transistor in the +5v, +12v, and - 12v circuits. A discrete regulator controls the current flow of the series pass transistor in the +73v circuit. Each regulator senses a change in output voltage of its circuit through a voltage divider. The circuit compares the change with a reference voltage and amplifiers this change to make the pass transistor maintain a constant output voltage.

If a short circuit occurs in the load of any power supply, a current-limiting transistor in the power supply's regulator circuit becomes forward biased. The result is a reduction of the current through the series-pass output transistor. This, in turn, reduces the output voltage.

In the +5v regulator circuit, an overvoltage-protect circuit limits the current if the voltage rises beyond a predetermined value. If the output voltage rises above 6.2v, a sense circuit turns on a silicon-controlled rectifier (SCR) which causes the regulator to limit the output current. In this same regulator, if one of the two series-pass transistors shorts, the SCR causes the fuse in the collector circuits of the transistors to open.

Figure 2-6 shows the effect of the foldback current limiting. Circuit design provides that when a predetermined current limit (150%) is reached, the current begins to decrease (foldback).

A protective ground line connects to the frame of the terminal and is tied to ground through the a-c power system.

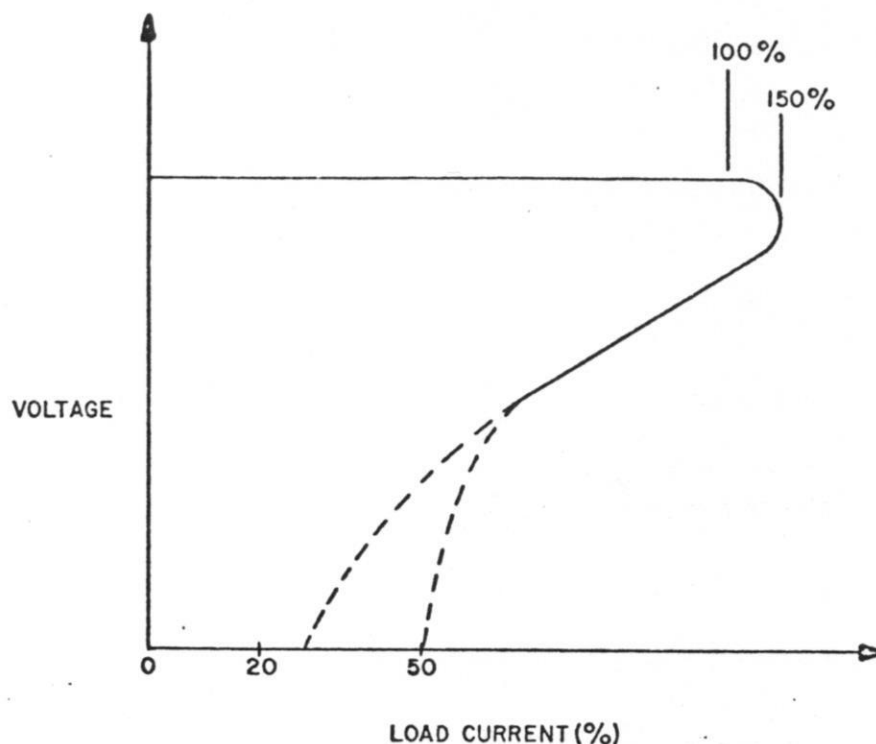


Figure 2-6. Foldback Under Full-Load to Short-Circuit Current

OPERATOR CONTROLS AND INDICATORS.

Table 2-3 describes the operator controls and indicators provided with the terminal. Figures 2-7 and 2-8 locate each of them.

TABLE 2-3. OPERATOR CONTROLS AND INDICATORS

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
POWER	Pushbutton Switch/Ind.	Operator Control Panel	Applies primary power to terminal when illuminated. Application of primary power sets all logic elements to initial or starting condition.
Brightness	Rotary Potentiometer Switch	Front Panel	Allows adjustment of video intensity used in the display. CCW: Reduces intensity. CW: Increases intensity.
Keylock Switch	Key-Operated Lock-Switch	Front Panel	Provides a manual lock out to prevent the keyboard from generating input codes.

TABLE 2-3. OPERATOR CONTROLS AND INDICATORS (CONT)

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
Keylock Switch (cont.)			Transmit function of terminal disabled when keyboard locked out, however, receive and print functions stay active.
Keylock Indicator	Indicator Light	Front Panel (Above Keylock Switch)	Illuminated when keyboard disabled by Keylock Switch.
LOCAL	Pushbutton Switch/Ind.	Operator Control Panel	Disables transmit circuits of terminal when illuminated. Keyboard data then automatically passes to memory for display. Data from communications modem still allowed and takes precedence over keyboard originated data. Local mode is commonly used when testing the terminal.
FULL/HALF Duplex	2-position Slide Switch	Connector Panel	FULL: All keyboard generated codes routed directly to communications modem. Codes not stored in memory or displayed unless returned from remote equipment depending on remote equipment programming. LOCAL mode disables this function. HALF: All keyboard generated codes routed to the modem and the display memory for subsequent display. LOCAL mode disables transmit to the modem, but allows display.
SCROLL DISABLE	Pushbutton Switch/Ind.	Operator Control Panel	Disables display line scroll operation when indicator is illuminated.

TABLE 2-3. OPERATOR CONTROLS AND INDICATORS (CONT)

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
DSR	Indicator Light	Operator Control Panel	Illuminated when terminal modem indicates it has power on and is in the data mode. Must be on to receive data. For maintenance use to check presence of useable carrier signal from terminal.
CTS	Indicator Light	Operator Control Panel	Illuminated when modem activates "clear-to-send" line. Must be on to start transmit. For maintenance use to check modem condition for transmit to modem.
BAUD RATE	4-position Rotary Switch	Connector Panel	Allows operator to select data transfer/receive rates between terminal and communications line. 75, 110, 150, 200, and 300 bits-per-second available.
PARITY SW	3-position Slide	Connector Panel	EVEN: Data words transmitted with even parity and checked for even parity when received. ODD: Data words transmitted with odd parity and checked for odd parity when received. Center Position: Parity disregarded.
Bell Tone	Audible Tone	Internal	Sounds when cursor enters 73rd character position of any display line to indicate approaching end of line. Sounds if Bell code (007₈) generated from keyboard or received from communications line.

TABLE 2-3. OPERATOR CONTROLS AND INDICATORS (CONT)

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
Keyboard Keys	Magnetic-Reed, Momentary-Contact Switches	Keyboard Panel	Enable operator data entry for message composition. Also enable teletypewriter special communications functions. See Data Entry Keyboard, this section, for details.
PRINTER ON LINE	Pushbutton Switch/Ind.	Operator Control	For use with hardcopy printer. Illuminated position activates hardcopy printer channel, then all communications as received or transmitted are printed if printer is connected with terminal. When not on (light out), PRINT key on keyboard must be depressed to obtain desired hardcopy of displayed data.
PRTR BSY	Indicator Light	Operator Control Panel	For use with hardcopy printer. When illuminated, indicates printer is busy with this terminal or another one sharing printer (8 terminals may share 1 printer). If PRINT key or PRINTER ON LINE key is depressed while PRTR BSY is lit, a new print operation does not occur. A print operation may be initiated only after PRTR BSY extinguishes.
PRTR ACT	Indicator Light	Operator Control Panel	For use with hardcopy printer. Illuminated only when terminal is transferring data to printer or has exclusive control of printer via the printer-on-line mode.

TABLE 2-3. OPERATOR CONTROLS AND INDICATORS (CONT)

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
PRINT Key	Magnetic-Reed Momentary-Contact Switch	Keyboard Panel	For use with hardcopy printer. With printer off-line and not busy (see above), depressing PRINT key sets cursor to start of displayed video page and advances cursor through entire display. During this time, entire page displayed transfers to printer. This print operation disables any data entry operations from keyboard or from modem and disables transmit to modem. Receiving data aborts the print operation.

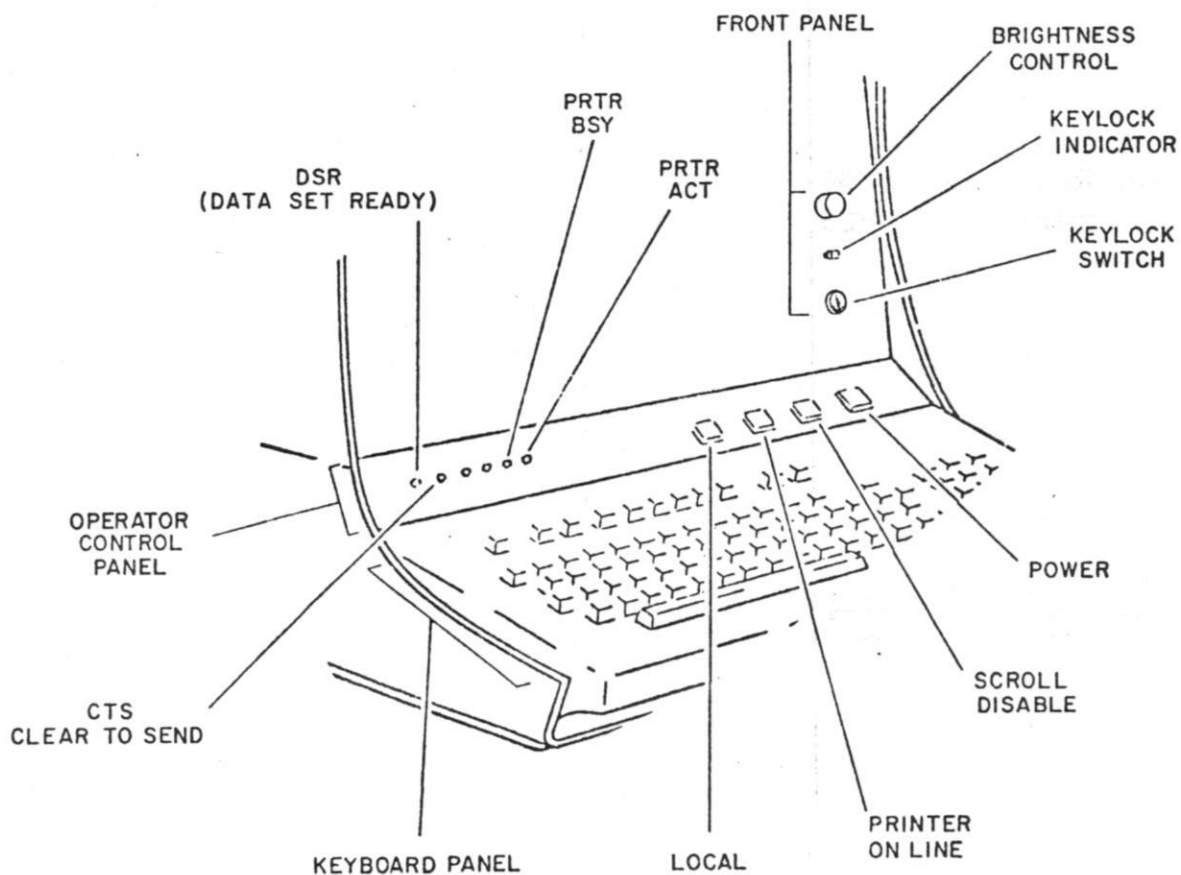


Figure 2-7. Front, Operator Control, and Keyboard Panel Controls

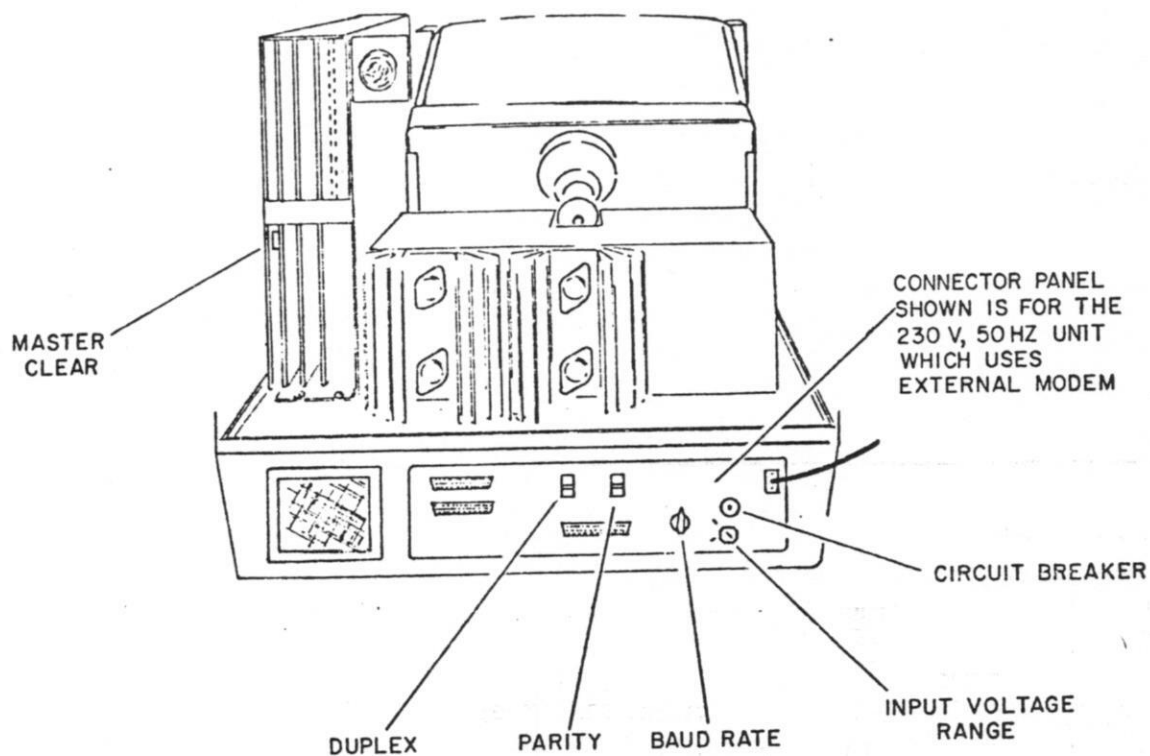


Figure 2-8. Connector Panel Controls

MAINTENANCE CONTROLS AND INDICATORS.

Table 2-4 describes terminal controls and indicators provided for maintenance use.

APPLYING POWER TO TERMINAL.

To apply power to the terminal, use the following procedure.

- 1) Depress the POWER switch/indicator (it should light).
- 2) Wait 30 seconds for cursor to appear on the viewing screen.

TABLE 2-4. MAINTENANCE CONTROLS AND INDICATORS

CONTROL OR INDICATOR	TYPE	LOCATION	FUNCTION
DSR	Indicator Light	Operator Control Panel (see fig. 2-7)	Illuminated when terminal modem indicates it has power on and is in the data mode.
CTS	Indicator Light	Operator Control Panel (see fig. 2-7)	Illuminated when modem activates clear-to-send line (see Modem Interface, this section).
MASTER Clear	Pushbutton Switch	Interface Card (see fig. 2-8)	Depressing clears internal circuits to initial or starting logic condition.
INPUT VOLTAGE RANGE	Two-position Rotary Switch	Connector Panel (see fig. 2-8)	Matches terminal power supply to 50 Hz input power source. NORMAL: for 210 to 256 VAC power source. LOW LINE: for 187 to 230 VAC power source.

- 3) If brightness of viewing screen is too bright/dim adjust Brightness knob as necessary (terminal should not operate with excessive display screen brightness or displayed information will be distorted and the life of the CRT display tube may be shortened).
- 4) With keyboard unlocked, and LOCAL mode set, depress several alphanumeric keys to check display.
- 5) If the cursor does not appear after checking brightness per step 3 above, push the red circuit breaker on the connector panel, re-apply power. If the cursor still does not display or if key depressions for characters or cursor controls fail to display, see Fault Isolation, Section V, this manual.

DATA ENTRY.

The display screen contains a cursor (position marker) that indicates where the next character will display on the screen. The cursor is a blinking underline below a character position and it blinks at approximately four times a second. In typical operation, when a character key is depressed, the character shown on the key displays above the cursor on the display screen. The cursor then advances to the next character position to show where the next character will display.



Blank display
with cursor



display after
depressing character
a key



display after
depressing a
and b character
keys

NOTE

The cursor and displayed characters appear as white forms on a black background unless contained in an inverse video field (see Inverse Video, this section).

In a typical operation (with display screen cleared), the cursor is under the first character position in the top line. As each character is entered from the keyboard, the cursor moves one character position to the right. As the cursor is advanced from the 72nd position of any line to the 73rd, an audible tone will sound indicating the proximity of the end of the line. When the end of the line is reached (80 characters), the cursor automatically moves to the first character position of the next line down. This process may continue until the last character position of the last line (line 8 in basic machine and line 16 in expanded option) is reached. At this time, if the machine is in scroll format mode, an additional input causes all lines on the display screen to move up one line position. The top line on the screen disappears and the cursor moves to the beginning of the new blank bottom line (see Figure 2-9). This is called a scroll effect. When the last character position of the bottom line is reached again, the scroll effect occurs again. If the machine is not in scroll format mode, when the last character position of the last line is used, the cursor automatically returns to the first character position of the top line. Remember this is only an example of operation. The cursor may be moved up, down, forward, and backward from the keyboard without displaying data. The display screen may be cleared at any time to display new data.

REQUEST FILE RECORDS FOR 0800 THROUGH 1000 FOR ANY A102309, A102343, OR A102440.

FILE NAME: GOODROE

RECORD 1	A102309	CODE M,N
RECORD 2	A102343	CODE NONE
RECORD 3	A102440	

ALSO LIST ANY OTHER ITEMS PERTAINING TO THIS FILE OR CODE.

CLASSIFICATION: NONE

REMARKS: SEND HASLO CODE M,N,T,Y

SCROLL MODE + DEPRESS



Note: Any Key Input Which Advances the Cursor from Last Position in Last Line.

FILE NAME: GOODROE

RECORD 1	A102309	CODE M,N
RECORD 2	A102343	CODE NONE
RECORD 3	A102440	

ALSO LIST ANY OTHER ITEMS PERTAINING TO THIS FILE OR CODE.

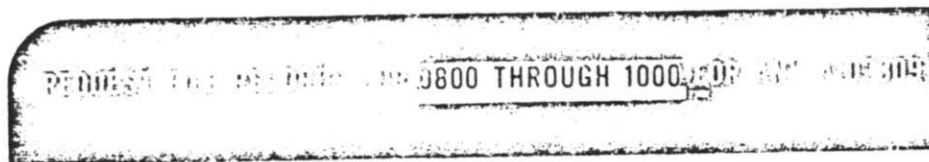
CLASSIFICATION: NONE

REMARKS: SEND HASLO CODE M,N,T,Y

Figure 2-9. Display Scroll Operation (8 Line Basic Display)

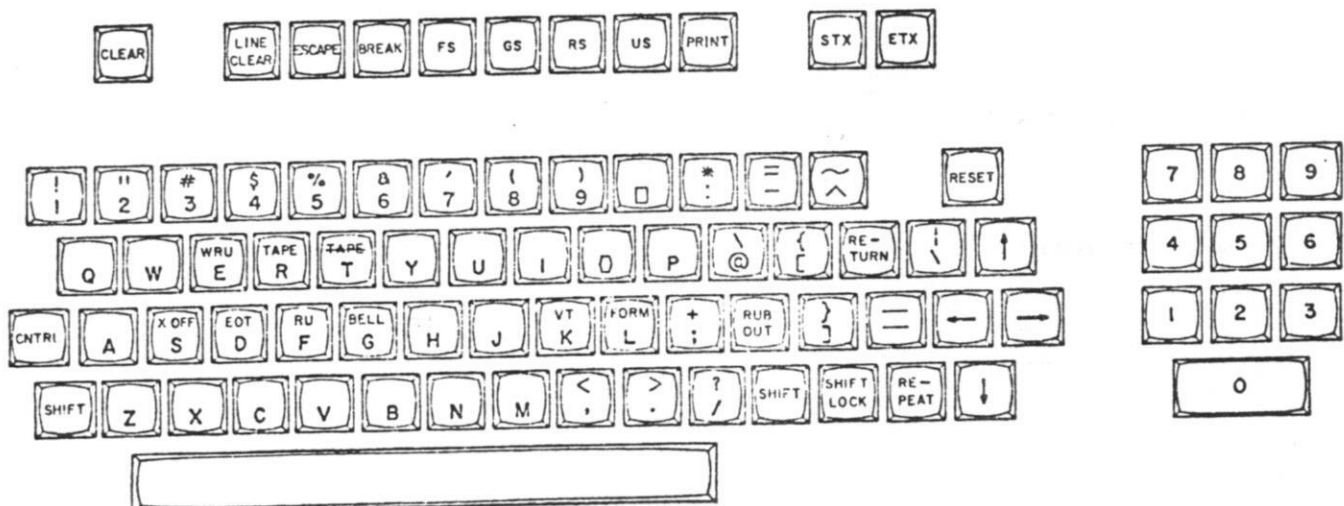
INVERSE VIDEO.

A specific coding allows for inversion of video in specific areas of a displayed message. A special code to start inverse video field and one to end the field can be generated from the keyboard or received from remote equipment via the communications modem. That portion of the displayed data that includes these start and end codes appears as black symbols on a white field. There are no limitations as to the location, number of inverse video areas, or to the total area that may be inverted. The start inverse video code (016_g) is generated from the keyboard by depressing the CNTRL key in conjunction with the N character key. The end inverse video code (017_g) is generated from the keyboard by using the CNTRL key with the letter "O" character key.



DATA ENTRY KEYBOARD.

The keyboard contains 48 alphanumeric/symbol keys, a cluster of 10 numeric keys, 5 keyboard control keys, and nineteen special function keys. Depressing any character or function key causes generating of a unique 7-bit USASCII-X3.4-1968 compatible code assigned by hardware to that key (see Tables 2-1 and 2-2). If a second character or function key is depressed while one key is still down, the second key does not interfere with the first key. The second key produces its code only after the first key is released.



Whenever the terminal is set for LOCAL operation, regardless of the Duplex mode setting (HALF or FULL), all codes generated by key depressions flow through the interface circuits to the control circuits. The control circuits hold the beam blank/unblank information necessary to display each character. They also keep track of all displayable data entry points and the location of the cursor. If a displayable character or function key entry is made, the control circuits direct the TV module with the correct video pulses for display entry or change. The LOCAL operation mode provides a convenient method to check operation of the keyboard and video display independent of the communications system that the terminal interfaces with. However, it should be kept in mind that the terminal will still receive data from the modem while operating in the LOCAL mode.

If the terminal is set in Remote operating mode (LOCAL indicator extinguished) and the Duplex mode switch is set for HALF, all codes generated by key depressions travel to control logic and the TV module for possible display as described in the preceding paragraph, however, the codes also transmit via the interface circuits to the modem for communication to remote equipment (eg; central processor). The terminal will receive data in this operating condition also.

When the terminal is set for Remote operation and the Duplex switch is set for FULL, all keyboard initiated codes transmit via the interface circuits directly to the communications modem for presentation at remote equipment. In this communications condition, all displayable operations must be returned from remote equipment before display can occur.

The various keys available for displaying data, moving the cursor, clearing the screen, etc. are described in detail in the Operator's Guide for this terminal.

OPTIONS.

This portion of the manual describes options that may be used with the terminal. If the equipment does not use an option, disregard this portion of this manual.

- OPTION 1 16 line x 80 character Display Format
- OPTION 2 Receive-Only Hardcopy Printer

16 x 80 DISPLAY FORMAT OPTION.

The terminal is designed to accept a character memory expansion of 640 additional characters thus enabling 16 lines of 80 characters on the video display as compared with the basic version with 8 lines of 80 character spaces (see Figure 2-10).

REQUEST FILE RECORDS FOR 0800 THROUGH 1000 FOR ANY A102309, A102343, OR A102440.

FILE NAME: GOODROE

RECORD 1	A102309	CODE M,N
RECORD 2	A102343	CODE NONE
RECORD 3	A102440	

ALSO LIST ANY OTHER ITEMS PERTAINING TO THIS FILE OR CODE.

CLASSIFICATION: NONE

REMARKS: SEND HASLO CODE M,N,T,Y

Standard 8x80 Display

REQUEST FILE RECORDS FOR 0800 THROUGH 1000 FOR ANY A102309, A102343, A102440
A103147, A103200, OR A104339

FILE NAME: GOODROE

RECORD 1	A102309	CODE M,N
RECORD 2	A102343	CODE NONE
RECORD 3	A102440	CODE M,N,T,Y
RECORD 4	A103147	CODE T,Y
RECORD 5	A103200	CODE NONE
RECORD 6	A104339	CODE NONE

ALSO LIST ANY OTHER ITEMS PERTAINING TO THIS FILE OR CODE.

CLASSIFICATION:	RECORDS 1,2	4A
	RECORD 3	2A
	RECORD 4	NONE
	RECORD 5	2A
	RECORD 6	NONE

REMARKS: SEND HASLO

Optional 16x80 Display

Figure 2-10. Optional 16 x 80 Display

This expansion is merely a "plug-in" addition of a second character memory printed circuit card and connecting cable as shown in Figure 2-11 (Expanded Memory Kit, see Foreword). If this option is used, the two character memory cards, being identical, are fully interchangeable. This expansion is easily added as an on-site change if ordered by a customer after receiving the basic terminal. This option does not affect the operation of the basic terminal, as described in the preceding portion of this manual, except that additional data can be displayed on the terminal view screen.

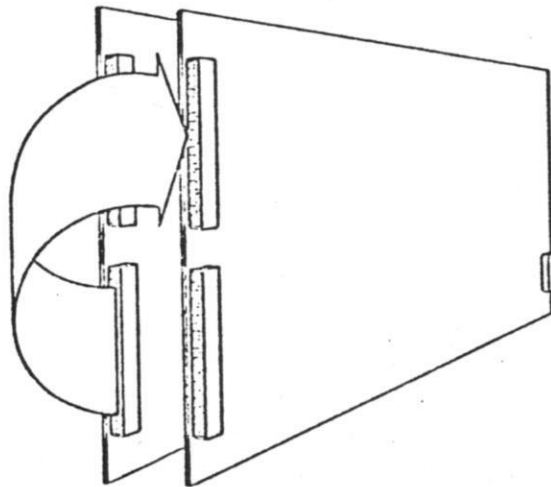


Figure 2-11. Expanded Memory Kit

RECEIVE-ONLY HARDCOPY PRINTER OPTION.

Housed in a separate cabinet, the optional hardcopy printer (see Figure 2-12) will operate with the basic terminal as a terminal containing any of the previously described options. This option enables obtaining hardcopy of messages either received or composed at a Conversational Display Terminal. Up to eight Conversational Display Terminals may share a single hardcopy printer. For complete descriptions of the printer interface and operator controls included in the terminal see "Printer Channel" paragraph this section. Also see "Printer On Line", "PRTR BSY", "PRTR ACT", and "PRINT Key" descriptions in Table 2-3. Operation, functions, and on-site maintenance of a hardcopy printer are described in manuals specifically for the particular printer unit. The printer option does not affect internal operation of the terminal (with or without options) except for communication via the "Printer Channel I/O Signals" (see description of this section).

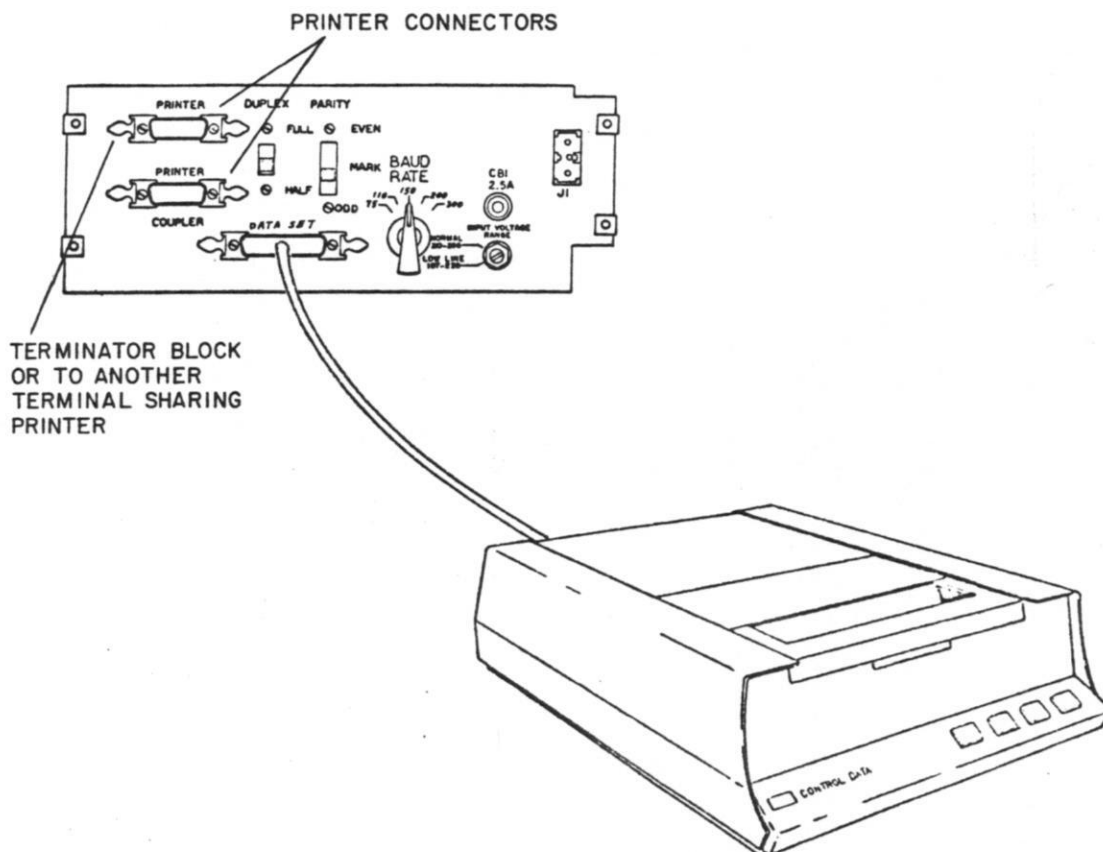


Figure 2-12. Hardcopy Printer Connection

SECTION III

INSTALLATION AND CHECKOUT

This section provides information vital to installation and checkout of the Conversational Display Terminal. Power requirements and cabling connection information is included.

CRATING.

When crating the terminal for shipment, use instructions and materials specified by Control Data Corporation Packaging Instructions, document number 59109100. This is available from:

Control Data Corporation
Materials Services, HQS07C
8100 34th Avenue South
Bloomington, Minnesota 55440

Figure 3-1 illustrates the shipping packaging for the terminal.

UNCRATING.

Refer to Figure 3-1 and uncrate the terminal as follows:

- 1 - Open the shipping container and carefully remove the terminal.
- 2 - Carefully remove all exterior packing material (plastic dust cover, shipping pallet, etc.) insuring that the viewing screen is not damaged.
- 3 - Place terminal on a sturdy, level-surfaced desk, counter, or table intended as the work station. Ensure that adequate surface area and rigidity is provided to safely support the terminal.

CAUTION

Two men recommended for lifting.
Avoid stress on terminal hood when
lifting or damage may result.

PHYSICAL LIMITATIONS.

Since the terminal is designed to sit on and operate from any sturdy flat-surfaced desk or counter top, mounting patterns are not of concern for installation. Installation is merely a task of placing the terminal on the desired work surface (see "Dimensions", Section I). A minimum of 6 inches (15 cm.) clearance must be maintained at the back of the terminal to provide adequate ventilation and cable clearance.

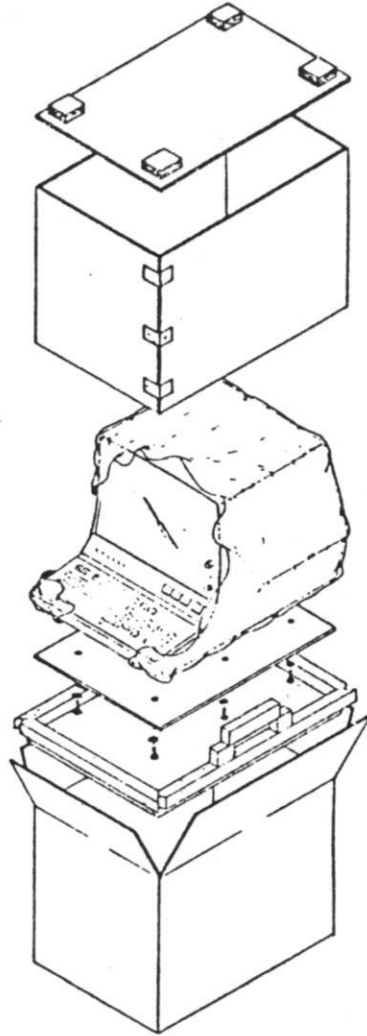


Figure 3-1. Terminal Packaging

POWER REQUIREMENTS.

Primary power cable requirements are as follows:

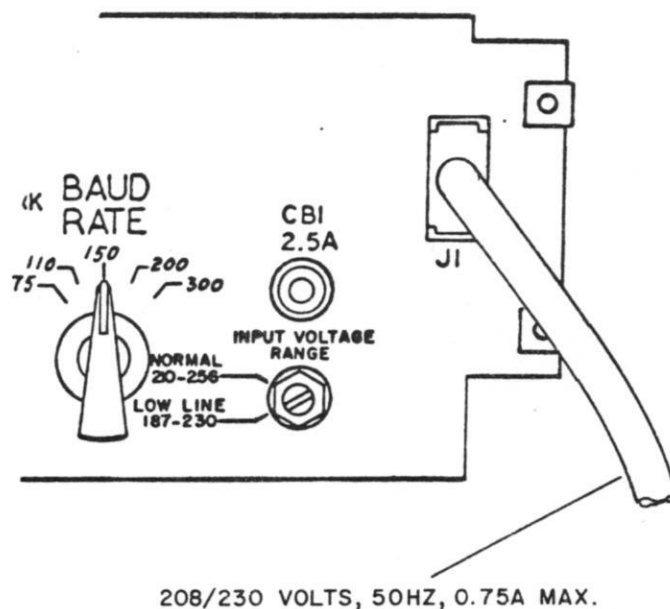


Figure 3-2. Power Requirements

COOLING & ENVIRONMENTAL REQUIREMENTS.

Cooling requirements are predetermined by the internal fan and the need for 6 inches (15 cm.) minimum clearance for ventilation at the back of the terminal. Environmental requirements are described in Section I.

PREPARATION FOR USE.

Before mounting the terminal in the desired work station, refer to "Cabinet Hood" removal procedure in Section VI and remove hood. Refer to Figure 3-3 as necessary and prepare the terminal for use as follows:

- 1 - Remove foam shipping block.
- 2 - Untape CRT connector and connect it to CRT.
- 3 - Remove tape CAREFULLY from display screen - DO NOT SCRATCH SCREEN.
- 4 - Inspect components of terminal to ensure that all components and connectors are properly seated. If necessary, verify module and other assemblies per the information provided in Section VII, Spare Parts Catalog.

Before replacing the hood check that the "Strap Option" jumpers within the display logic module are placed correctly for the particular communications system. Refer to Figure 3-4 and perform the following:

- 1 - Remove all screws ① holding display logic module side-plate ② and rear card retainer strap ③.
- 2 - Gently, to avoid damaging printed circuits, remove side-plate to make strap option jumpers S1, S2 and S3 ④ accessible.
- 3 - Refer to Table 3-1 and check jumper placement. Adjust jumpers if necessary (jumpers are hand press-fit: no soldering required).
- 4 - Replace side-plate by reverse of preceding steps 2 and 1.
- 5 - Replace cabinet hood. The terminal is ready for mounting in the work station.

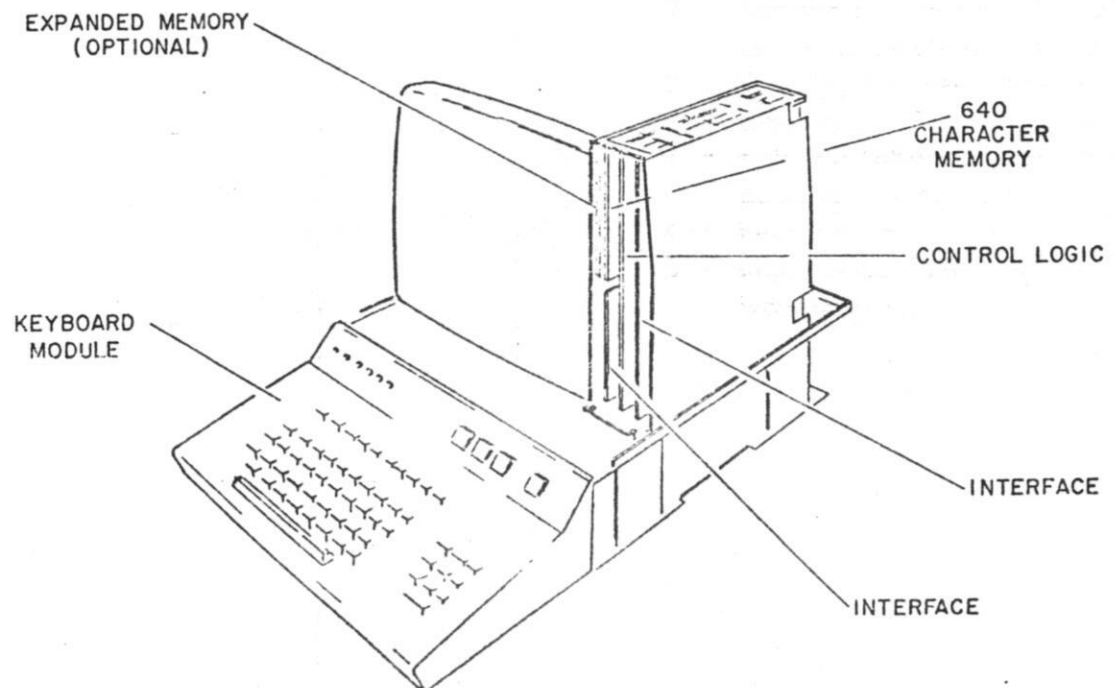
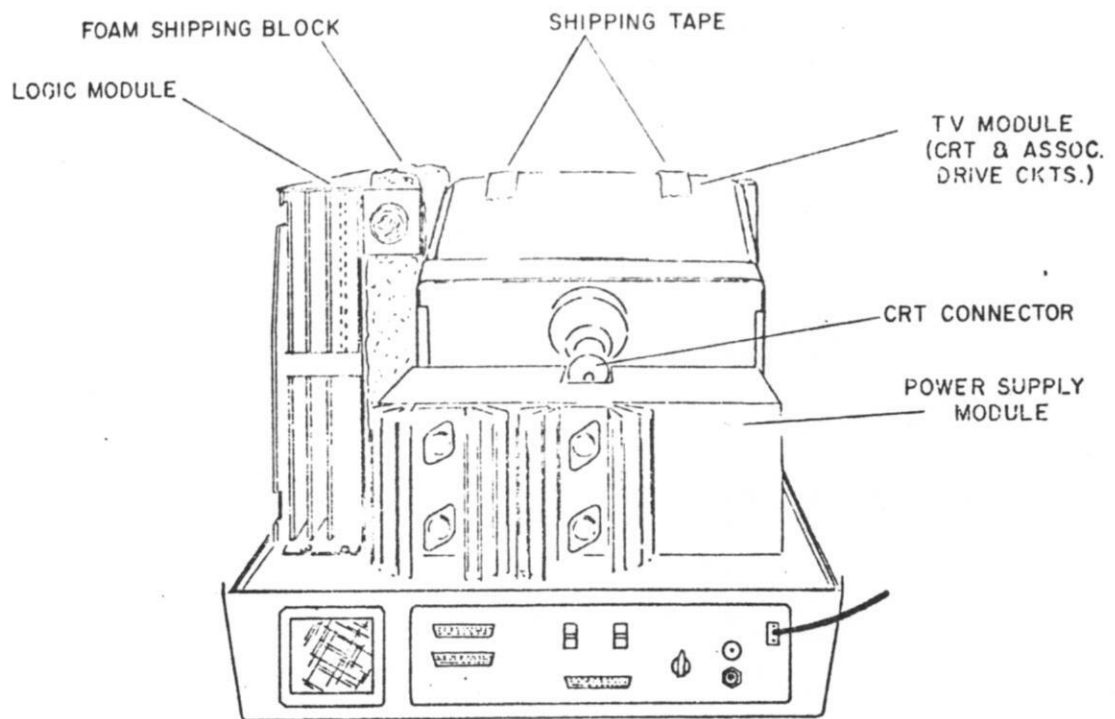


Figure 3-3. Internal Shipping Materials and Component Location

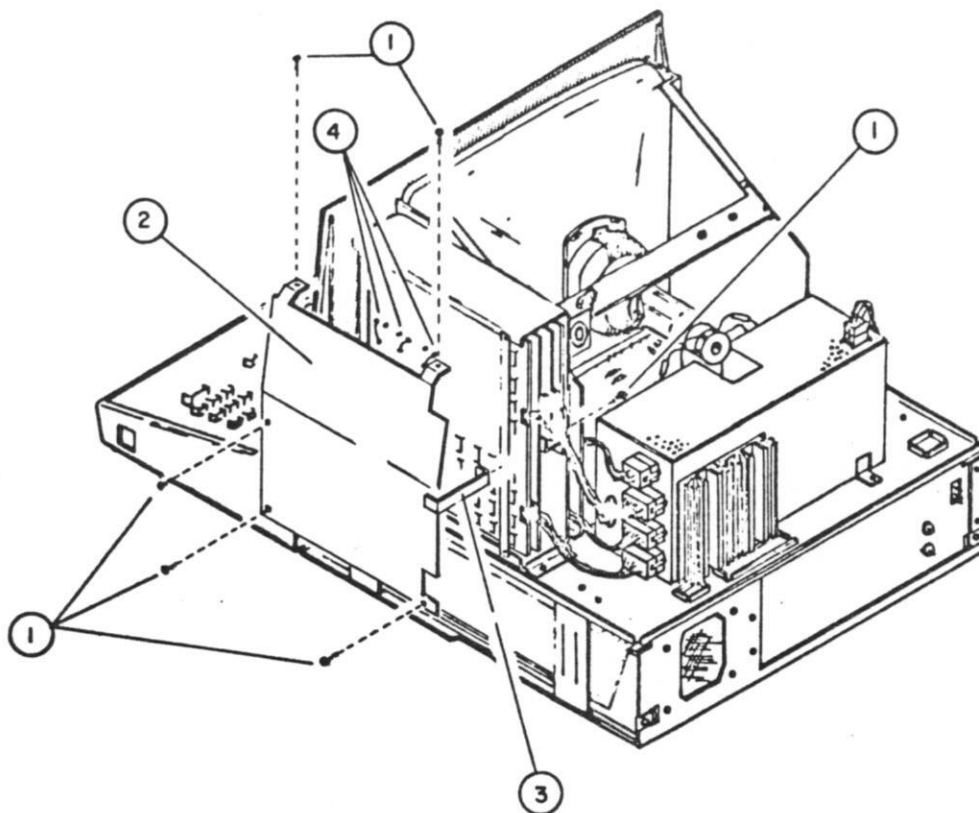


Figure 3-4. Strap Option Placement

TABLE 3-1. STRAP OPTION JUMPER FUNCTIONS

JUMPER STRAP	POSITION	FUNCTION
S1	RUB RUB	Rub Out codes (177_8) do not affect displayed data. Rub Out codes (177_8) cause a Rub Out character (■) to display.
S2	CONT BRK 2 CH BRK	Terminal transmits a continuous Break function while BREAK key is depressed. Terminal transmits a Break function of 2 character time duration for each BREAK key depression.
S3	CONT DTR LOC DTR	Terminal sends a Data Terminal Ready signal to the modem interface whenever POWER is on (indicator illuminated). Terminal sends a Data Terminal Ready signal to the modem interface only when in Remote operating mode (LOCAL indicator extinguished).

MOUNTING PROCEDURES — BASIC TERMINAL.

Mount the terminal in the desired work station per the following steps.

- 1 - Place the unit on a sturdy, flat-surfaced desk, counter, or table ensuring that adequate surface area and rigidity is provided to safely support the terminal.
- 2 - Connect site data set (modem) cable to connector labeled "DATA SET" on connector panel (maximum modem-to-terminal cable length is 50 feet). Reference: Modem Interface Signals, Section II.
- 3 - Connect external a-c power cable to external power source available at the installation site.

Set the INPUT VOLTAGE
RANGE selector screw on the connector panel as follows:

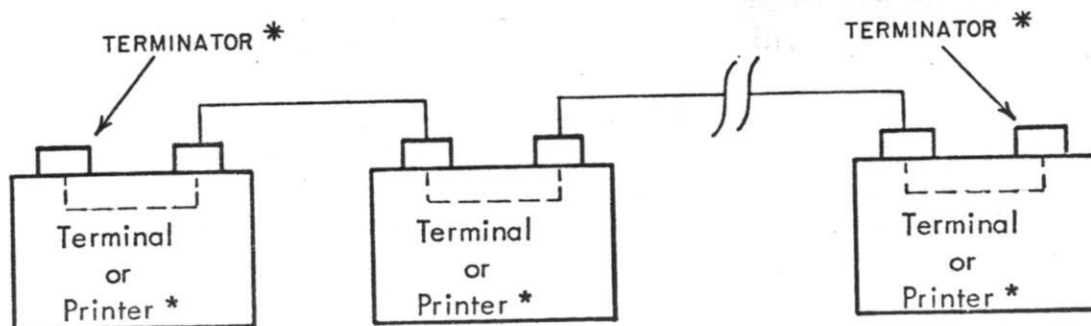
NORMAL	position for 210 to 256 VAC power source
LOW LINE	position for 187 to 230 VAC power source

- 4 - Depress POWER switch/indicator located on the operator's control panel to apply power to the terminal. Power is on when indicator is lit.

MOUNTING PROCEDURES - HARDCOPY PRINTER OPTION.

Mounting procedures for a hardcopy printer are contained in the Installation Instructions for the printer. The connections made with the Conversational Display Terminal are as follows:

- 1 - Connect printer cables to terminal connectors labeled "PRINTER" on connector panel. Figure 3-5 shows the required cable routing for terminals using a printer (maximum printer interface cable length, including any other terminals sharing the printer in "daisy chain" fashion, is 1500 feet or 458 meters). Reference: Printer Channel I/O Signals, Section II.



* From one to eight terminals may share one printer. Printer may be located between terminals on the interface line or on either end. Terminator blocks (part no. 62078900) must be installed on the spare connector of the device (terminal or printer) located on each end of the interface.

Figure 3-5. Terminal/Printer Cable Interface

CHECKOUT.

Checkout is an operational performance check and does not require any test equipment. Since the Conversational Display Terminal is designed to send and receive messages, successful execution of all intended communications formatting and receiving operations demonstrates proper operation of the terminal. Refer to the Operator's Guide and Hardware Programming Manual as necessary for operational descriptions. The following procedure is a typical operational performance check which may be done to check the terminal operation.

- With power on (POWER indicator lit) rotate Brightness control knob (on front panel) CW until the cursor (blinking underline) is visible in the display area. Brightness should not be set higher than necessary as this may reduce the life of the display tube.
- Unlock keyboard (KEYLOCK indicator extinguished — turn KEYLOCK keyswitch if necessary).
- Ensure that the terminal is in Local (test) operating mode by observing LOCAL switch/indicator on the operator control panel, if lit; the unit is in local mode, if not lit; depress LOCAL switch to light indicator.
- Disable the scroll format mode (SCROLL DISABLE switch/indicator lit — depress if necessary).
- Check keyboard and display operation for all displayable characters by depressing each alphanumeric key and observing results on the display screen (see Operator's Guide for the terminal for displayable character keys if necessary).
- Check keyboard and display operation for all edit function control keys while observing results with displayed data on the display screen (see Operator's Guide for the terminal for edit function keys if necessary).
- Check operation of keyboard control keys LOCK, SHIFT, and REPEAT (see Operator's Guide for the terminal for these keys if necessary).
- Fill entire display area with symbols "a" on top line, "b" on second line, "c" on third line, etc. (8 lines x 80 symbols with basic unit and 16 lines x 80 symbols with Expanded Memory Kit).
- Ensure that the cursor is in the last character position of the bottom display line.

- Depress DISABLE SCROLL switch/indicator, extinguishing light, to place terminal in scroll format mode.
- Depress Skip () cursor control key or space bar and observe display; scroll operation should occur (see Figure 2-9 in Section II).
- Fill new last line with any keyboard character(s) and observe display for scroll operation again as last character position in the bottom line is filled.
- Refer to the site system operating instructions, or have site personnel assist, and perform all required functions for the terminal, utilizing the CNTRL key and all special function keys (refer to the Operator's Guide for the terminal if necessary).

Remember, the above steps are a sample checkout procedure and may be modified as may appear useful at a particular site. If the terminal should fail to operate correctly, first check all cable connections with power cable removed, replace power cable and check operation again. If the terminal still operates incorrectly, refer to Section V, Fault Isolation for field corrective action.

WARNING

DANGEROUS HIGH VOLTAGE EXISTS WITHIN THE CIRCUITS OF THE UNIT WHEN POWER IS APPLIED. EXERCISE UTMOST CAUTION WHEN CHECKING CONNECTIONS EVEN WITH POWER TURNED OFF AND/OR POWER CABLE REMOVED SINCE CAPACITORS USED IN THE HIGH VOLTAGE VIDEO MODULE REMAIN CHARGED AT A HIGH LEVEL FOR SOME TIME AFTER POWER REMOVAL. SEE SAFETY WARNING PAGE 6-8, SECTION VI.

After verifying correct terminal operation during the preceeding checkout, installation and checkout of the unit is complete.

USER INSTRUCTIONS.

After terminal is installed and operational, inform user of the preventive maintenance tasks which are user's responsibility to help keep the equipment attractive and trouble-free. These tasks are described in the user's Operator's Guide.

SECTION IV

PREVENTIVE MAINTENANCE

Preventive Maintenance describes those tasks that should be performed during emergency maintenance by the one answering the emergency maintenance call. This maintenance consists of only light housekeeping tasks. No electrical or mechanical adjustments are required. Verify that the equipment operators/users have been performing the preventive maintenance tasks which are their responsibility (the first four items listed below).

To perform preventive maintenance on the Conversational Display Terminal perform the following:

- Remove dust from keyboard with a soft-bristled brush.
- Clean exterior of equipment with a damp, lint-free cloth.
- Clean face of display screen with a clean, soft cloth (any grit on cleaning cloth scratches viewing screen) and a mild glass-cleaning solution (name-brand aerosol or spray glass cleaners are suitable).
- Remove and clean blower air filter as necessary (filter removes from outside). Filter must be kept clean and unobstructed or display station may overheat. A water and soap solution is sufficient to clean air filter. Be sure filter is dry before replacing.
- If it becomes necessary to clean inside of display screen and face of CRT, remove the cabinet hood and the view screen face plate (see Remove and Replace Procedures, Section VI). This item is for experienced personnel action only.

SECTION V

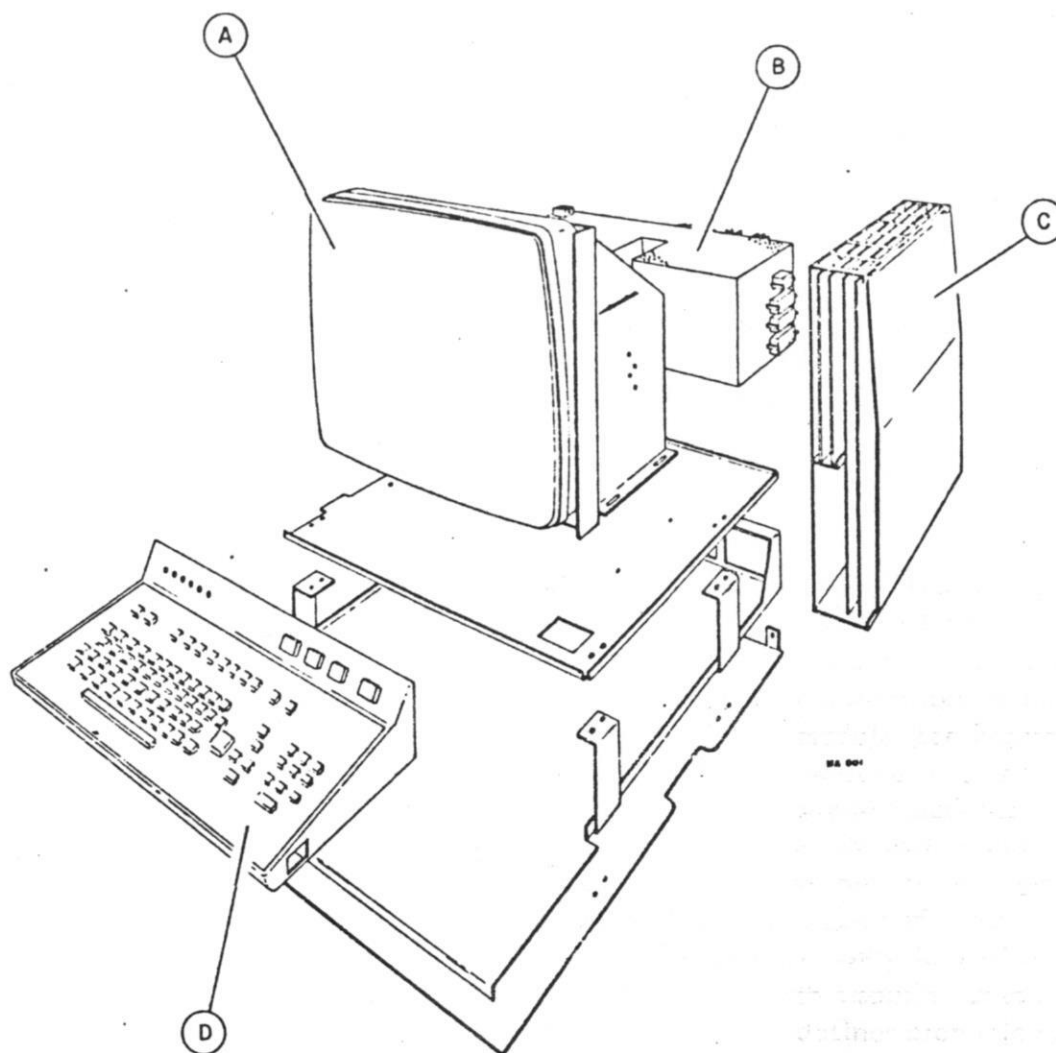
FAULT ISOLATION

This section serves as a fault isolation guide for correcting a malfunctioning Conversational Display Terminal located at a customer site.

FAULT ISOLATION PHILOSOPHY.

Due to the nature of the equipment and the variety of system applications, no fault isolation diagnostic programs apply to isolate faulty circuits within the terminal. The on-site maintenance approach for this equipment is to logically isolate malfunctions to the replaceable module level and remove and replace the faulty module (see Figure 5-1). This is done by observing terminal operation, noting any malfunctions, associating existing malfunctions to modular circuits, replacing the suspect modules, and then rechecking terminal operation. Section VII of this manual contains the applicable on-site spare parts catalog for the terminal. Since modules in the terminal are quickly and easily replaceable, it is desirable to replace modules as part of a process of elimination in order to isolate a fault rather than attempt lengthy logical analysis of the problem to locate a malfunction. For this reason, this section does not contain lengthy step-by-step isolation faulty modules. Table 5-1 defines probable causes for a variety of symptoms which may occur with a terminal. An understanding of probable causes for faults and of the module and inter-module is essential for logically isolating malfunctions to a particular module.

Before the reader must perform fault isolation for the terminal, it is recommended that he read Section I, General Description to acquaint himself with the function and purpose of the equipment and he should read Section II, Operation, to become familiar with the operation of the modules and controls which comprise a terminal.



- A VIDEO-DISPLAY (TV) MODULE
- B POWER SUPPLY MODULE
- C LOGIC MODULE
- D KEYBOARD MODULE

Figure 5-1. Display Station Modules

FAULT ISOLATION PROCEDURES.

When a fault occurs within the terminal, the first maintenance step should be to master clear the logic circuits by cycling power off and on to try to clear any logic circuit "hang-up" that may be causing the difficulty (see Figure 5-2). To master clear the terminal, perform the following:

- Depress POWER indicator/switch. POWER indicator is extinguished.
- Wait 30 seconds.
- Depress POWER indicator/switch. POWER indicator is illuminated.

If master clearing the terminal does not eliminate the problem, the next procedure for returning the unit to service should be a power supply module voltage check. Figure 5-3 shows how to check the fuse. Figure 5-4 locates external voltage test points for the power supply.

To check the display power supply voltage, perform the following:

- Refer to Corrective Maintenance, Section VI, for cabinet hood removal and remove hood.
- If voltage check at connectors is desired, place identifying tags on cables to power supply connectors J2, J3, J4 and J5 to insure proper reconnections and refer to Figure 5-4 and disconnect output connectors J2, J3, J4 and J5.
- Attach power cord to AC power connector to supply primary power to the unit (interlock power line disconnects when cabinet hood is removed).
- Depress POWER switch turning power on.
- Refer to Figure 5-3 and check fuse with multimeter.
- Use multimeter to test output of all connector pins or test at test points, whichever desired (see Figure 5-3). Go between ground pins and voltage pins.

If fuse or output voltage checkout produces a voltage deviation, at any point, of over 5%, the power supply module should be adjusted if possible. If not possible to adjust, then replace. Refer to Section VI for power supply adjustment and replacement procedures.

If checkout is normal, proceed with fault isolation per Table 5-1.

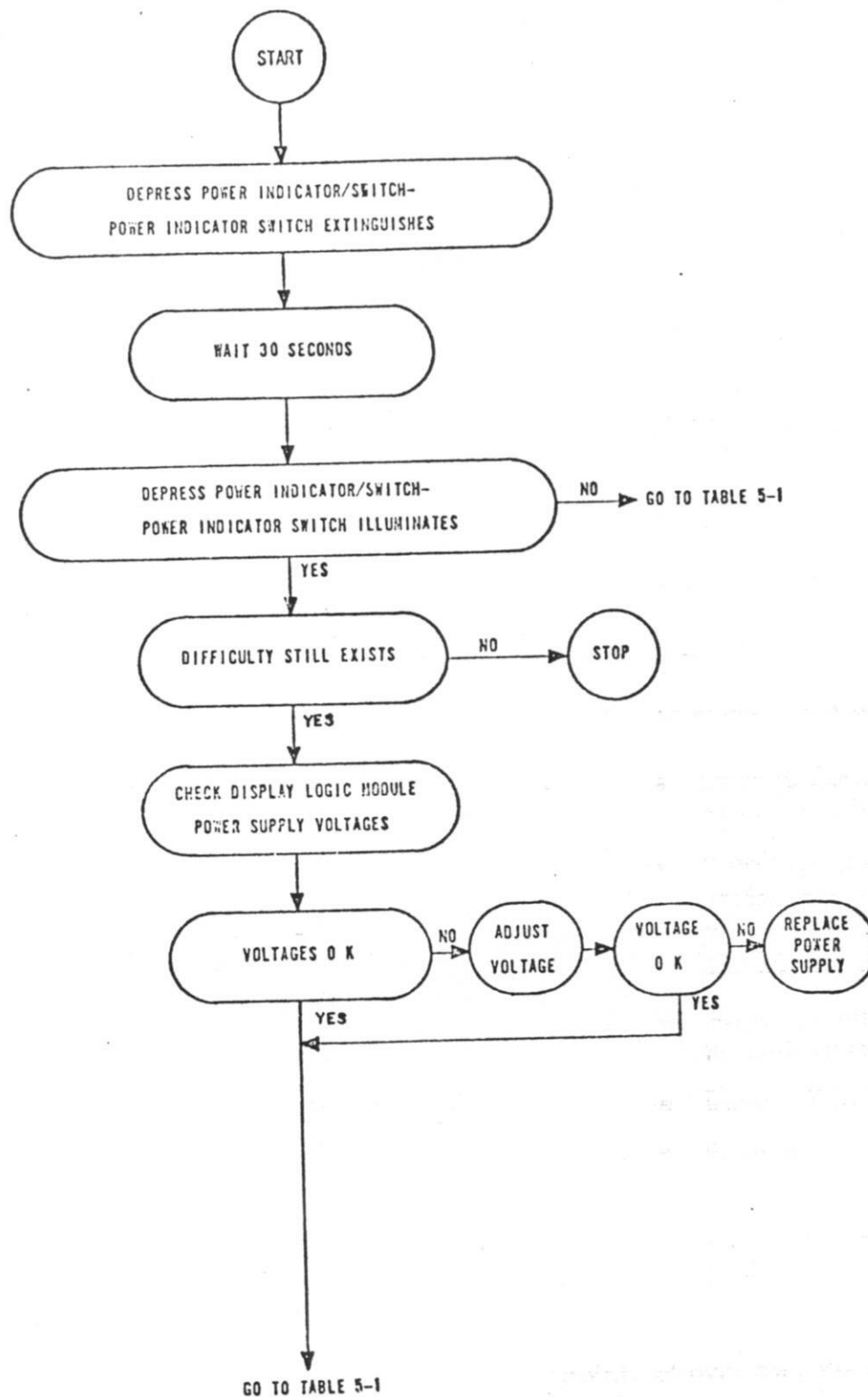


Figure 5-2. Fault Isolation Procedure

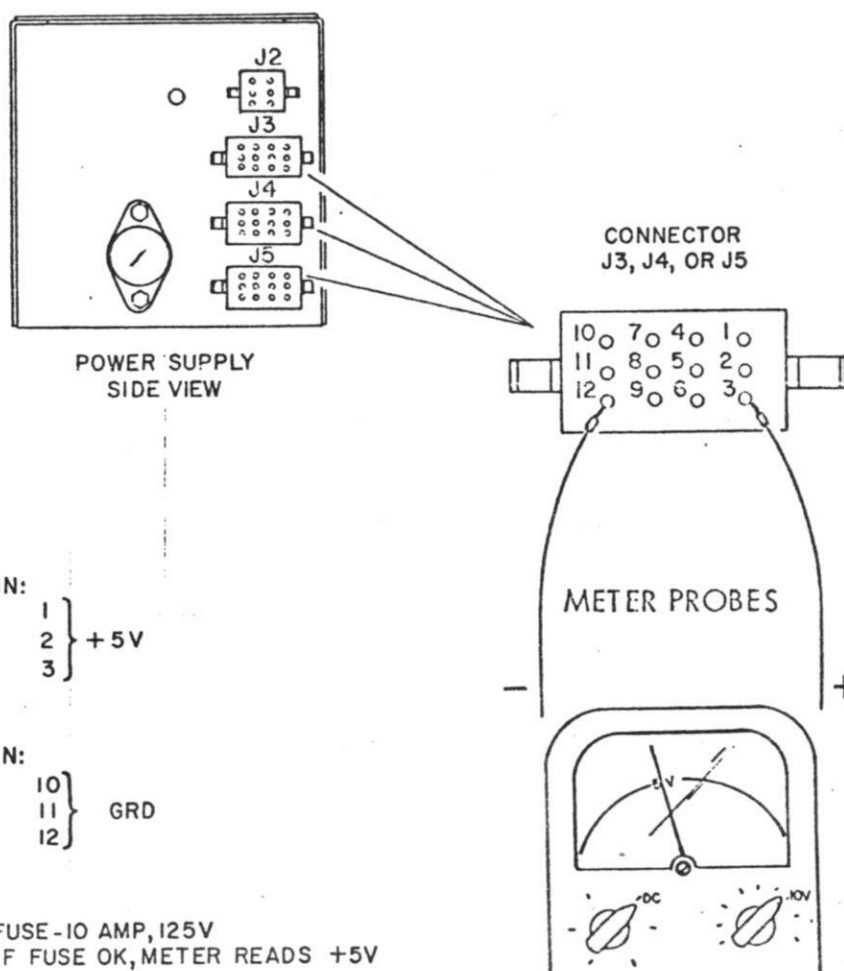
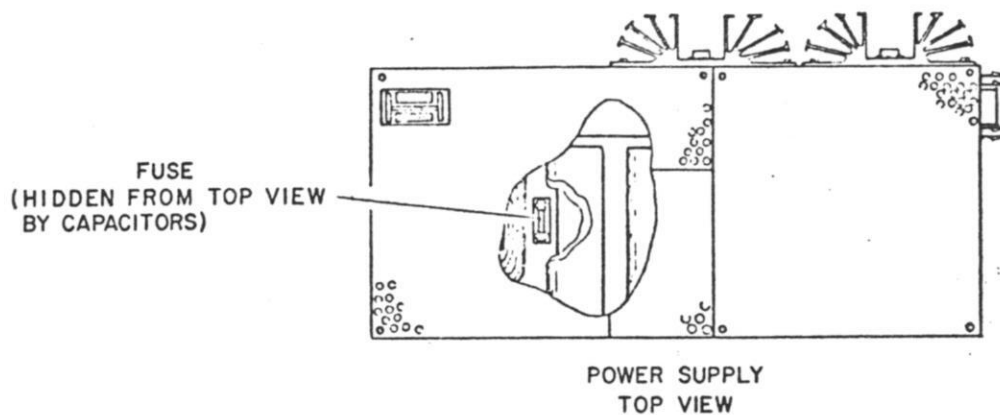


Figure 5-3. Fuse Checkout and Location

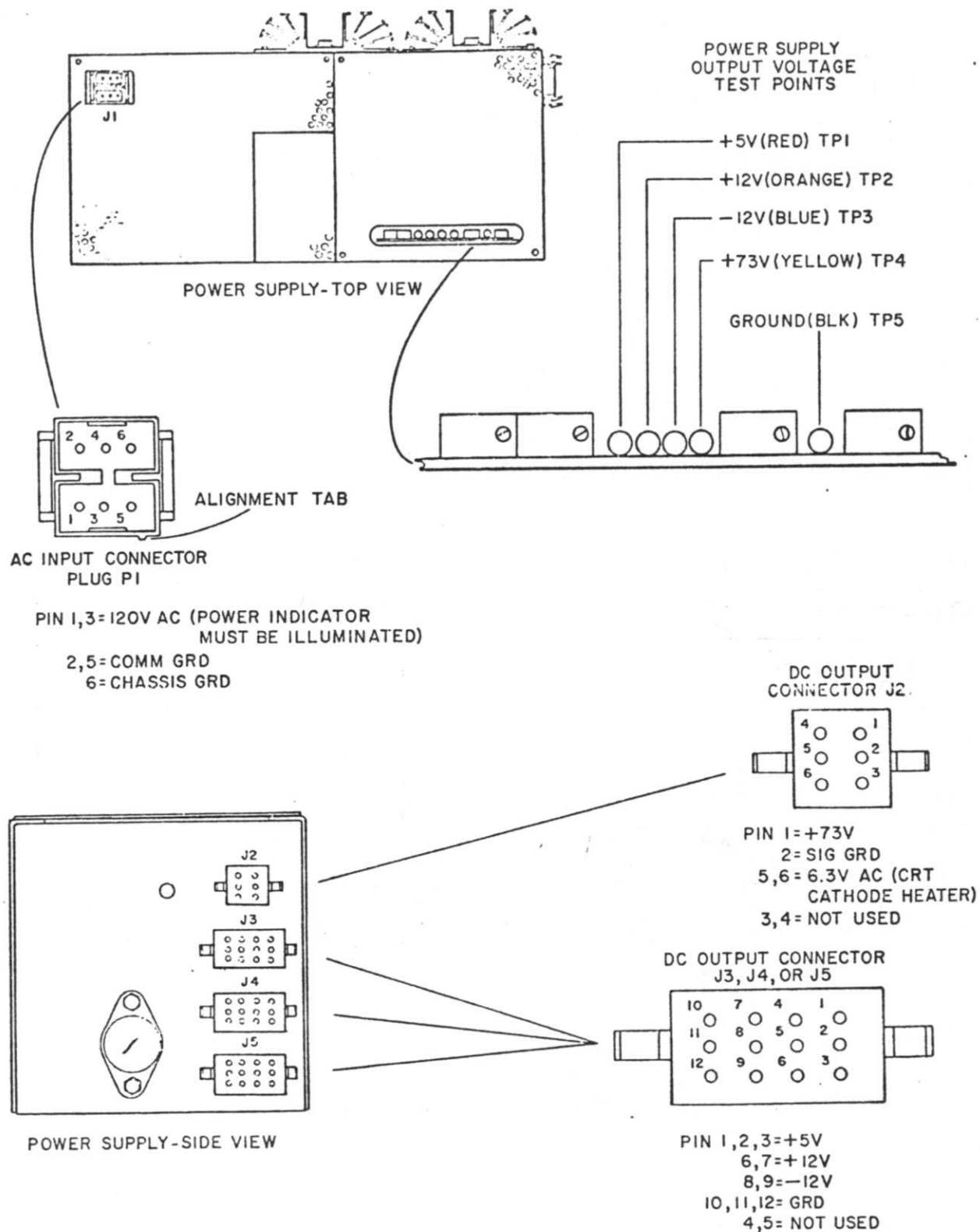


Figure 5-4. Power Supply Voltages

TABLE 5-1. FAULT ISOLATION CHART

SYMPTOM	CHECK OR PERFORM IN SEQUENCE SHOWN Note: Before isolating faults per this chart, master clear the terminal and check power supply output and fuse (see page 5-3). Before replacing any suspect module, check seating of all accessible plug-in subassemblies within the module. Also check interconnecting cables and connectors for visually apparent damage and firm seating.
Display is too bright or too dim.	(a) Adjust BRIGHTNESS control. (b) Replace TV module.
Poor Contrast	(a) Adjust Contrast control. (b) Replace TV module.
Display rolls vertically	(a) Adjust Vertical Hold. (b) Is vertical blanking bar present (see Figure 5-5). If yes, replace TV module. If not, replace logic module.
Display tears horizontally	(a) Adjust Horizontal Hold control. (b) Replace TV module. (c) Replace Logic module.
Poor Focus	(a) Adjust Focus control. (b) Replace TV module.
Display has insufficient height	(a) Adjust Vertical Size control. (b) Replace TV module.
Nonuniform height of all display lines.	(a) Adjust Vertical Linearity control. (b) Replace TV module.
Display has insufficient width.	(a) Not an on-site adjustment. (b) Replace TV module.
Nonuniform width of all symbol positions.	(a) Not an on-site adjustment. (b) Replace TV module.
Display is rotated clockwise or counterclockwise from vertical position.	(a) Adjust Yoke. (b) Replace TV module.

TABLE 5-1. FAULT ISOLATION CHART (CONT)

SYMPTOM	CHECK OR PERFORM IN SEQUENCE SHOWN
Display incorrectly positioned (too far left-right, or up-down.	(a) Adjust Raster Centering Tabs. (b) Replace TV module.
POWER indicator does not light, and cursor does not display.	(a) Is site power available. (b) Is terminal AC power cord plugged in? (c) Is AC power cord seated properly at rear of terminal. (d) Is circuit breaker located at rear of display station, set (pushed in)? (e) Is AC power cord damaged? Wires broken? Replace if necessary. (f) Replace POWER switch/indicator (see note). (g) Replace circuit breaker (see note).
No Cursor	(a) Is POWER indicator illuminated? If not, depress POWER switch, indicator illuminates. (b) Is raster visible when BRIGHTNESS control is turned up? (c) Is AC input power available? See (a) through (e) of preceding symptom. (d) Are DC output power cables from power supply module connected on both ends? (e) Is fuse f1 blown? (This can be determined by checking for +5v as shown in Figure 5-2. If no voltage, fuse is probably blown. (f) Replace logic module. (g) Replace TV module. (h) Replace power supply module.
No character will display. Cursor is visible. LOCAL mode.	(a) Is keyboard unlocked? (b) Replace logic module. (c) Replace keyboard module. <u>Note:</u> May require replacing next higher order assembly depending on spares available. See On-Site Spare Parts Catalog, Section VII.

TABLE 5-1. FAULT ISOLATION CHART (CONT)

SYMPTOM	CHECK OR PERFORM IN SEQUENCE SHOWN
No cursor and no character displays.	(a) Is BRIGHTNESS control turned down too far? (b) Replace logic module. (c) Replace TV module.
Keyboard does not unlock.	(a) Master clear display station by cycling power off and on with POWER indicator/switch. (b) Check wiring for keylock switch and replace switch if necessary (see note). (c) Replace logic module.
Any keyboard key does not work.	(a) Replace keyboard. (b) Replace logic module.
PRINT key or PRINTER ON-LINE switch/indicator does not cause printout for a terminal with associated printer.	(a) Is keyboard unlocked? (b) Check if PRTR BSY (see Table 2-3). (c) Check printer power. (d) Check printer interface connections. (e) Check printer operation and replace if necessary. (f) Replace logic module. (g) Replace keyboard if PRINT key or replace switch/indicator if PRINTER ON LINE switch (see note).
One or both modem indicators do not light.	(a) Check modem and telecommunications system connections. (b) If modem failing, replace. (c) Replace indicator (see note).
SCROLL DISABLE switch/indicator does not disable or enable scroll.	(a) Replace logic module. (b) Replace switch/indicator (see note).
FULL DUPLEX and On-Line (LOCAL Switch/Indicator extinguished) operation in error. (Failure of Echo-plex operation).	(a) Check PARITY switch setting. (b) Check BAUD RATE switch setting. (c) Check data set communications line connections. (d) Check data set (modem). (e) Check system operation. (f) Replace logic module. (g) Replace DUPLEX switch (see note). (h) Replace LOCAL switch/indicator (see note).

TABLE 5-1. FAULT ISOLATION CHART (CONT)

SYMPTOM	CHECK OR PERFORM IN SEQUENCE SHOWN
Displayed messages from remote site contain parity error characters.	(a) Check PARITY switch setting. (b) Check (b) through (f) of preceding symptom. (c) Replace PARITY switch (see note).
Displayed messages from remote site with missing or scrambled characters.	(a) Do (b) of preceding symptom.

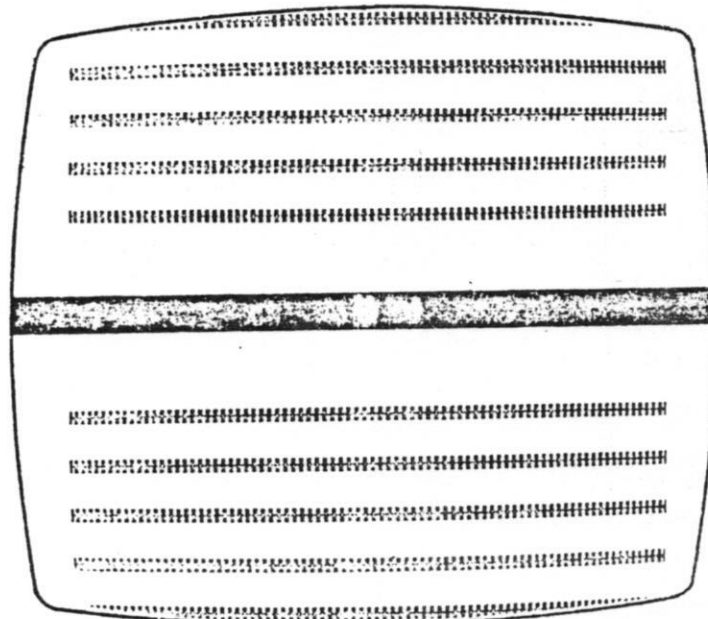


Figure 5-5. Vertical Blanking Bar (vertical hold adjusted so bar is visible)

SECTION VI

CORRECTIVE MAINTENANCE

Corrective maintenance for the terminal includes power supply module and TV module adjustments and removal and replacement procedures for the on-site replaceable parts. Corrective maintenance is performed by the serviceman as a result of fault isolation (see Section V).

POWER SUPPLY MODULE ADJUSTMENTS.

With the cabinet hood removed, the power supply output voltages may be measured. With the power supply installed and its cover in place, output voltages are checked at test points TP1 through TP5 or at connectors J2, J3, J4, and J5 (see Figure 6-1). The test points are available through an access slot in the perforated cover and they are recommended. Input voltage is checked at connector J1. When the power supply cover is in place (the power supply must be removed to remove the protective cover).

To adjust the DC output voltages of the power supply, perform the following:

- Apply power to power supply.

NOTE

Wait 15 minutes after applying power to power supply before proceeding.

- Set multimeter to read +73v.
- Connect negative test lead of multimeter to black test jack on top of printed-circuit board (see Figure 6-2).
- Adjust +73v potentiometer until multimeter indicates +73v.
- Remove test lead from yellow test jack and connect it to orange test jack (see Figure 6-2).

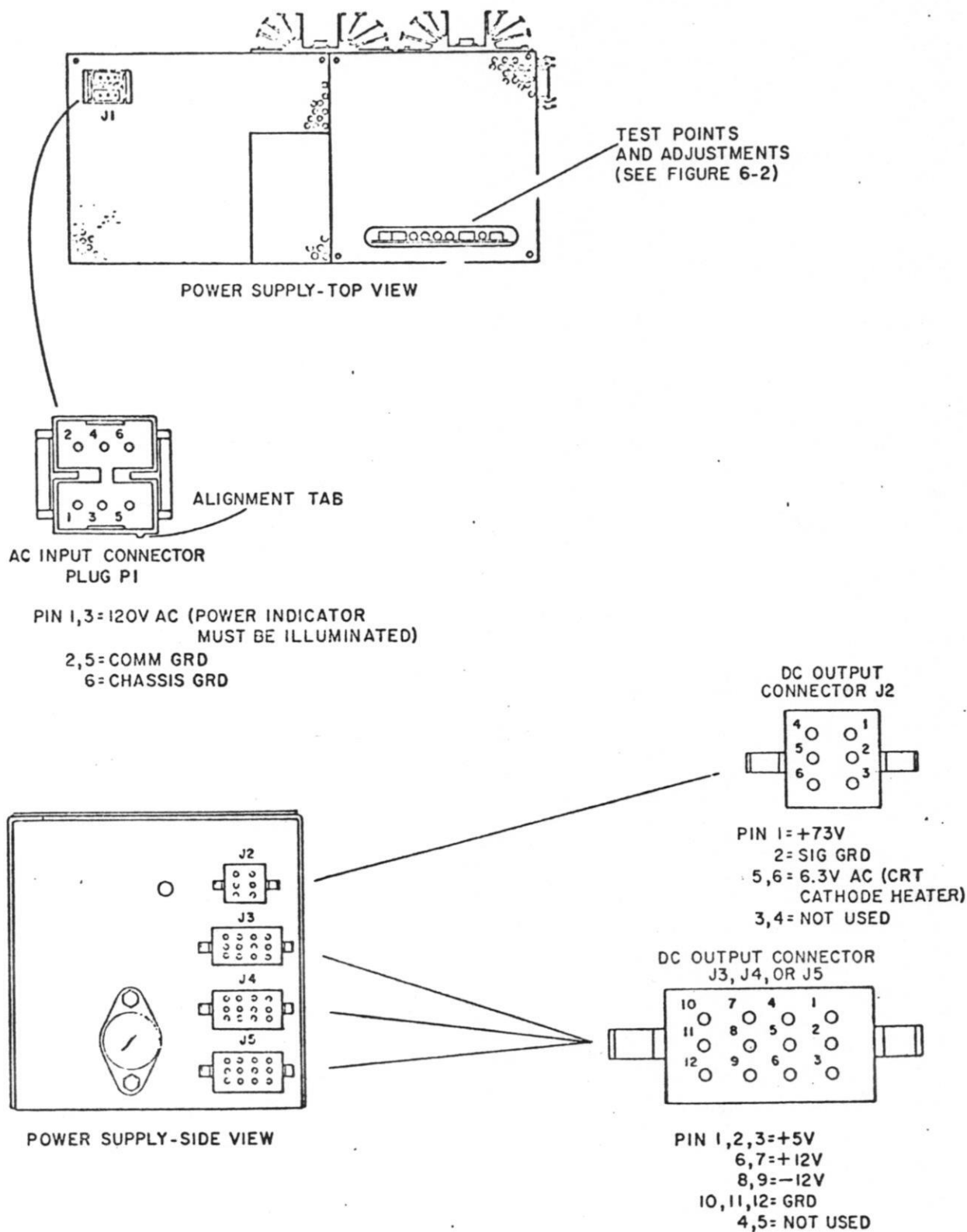


Figure 6-1. Power Supply Voltages

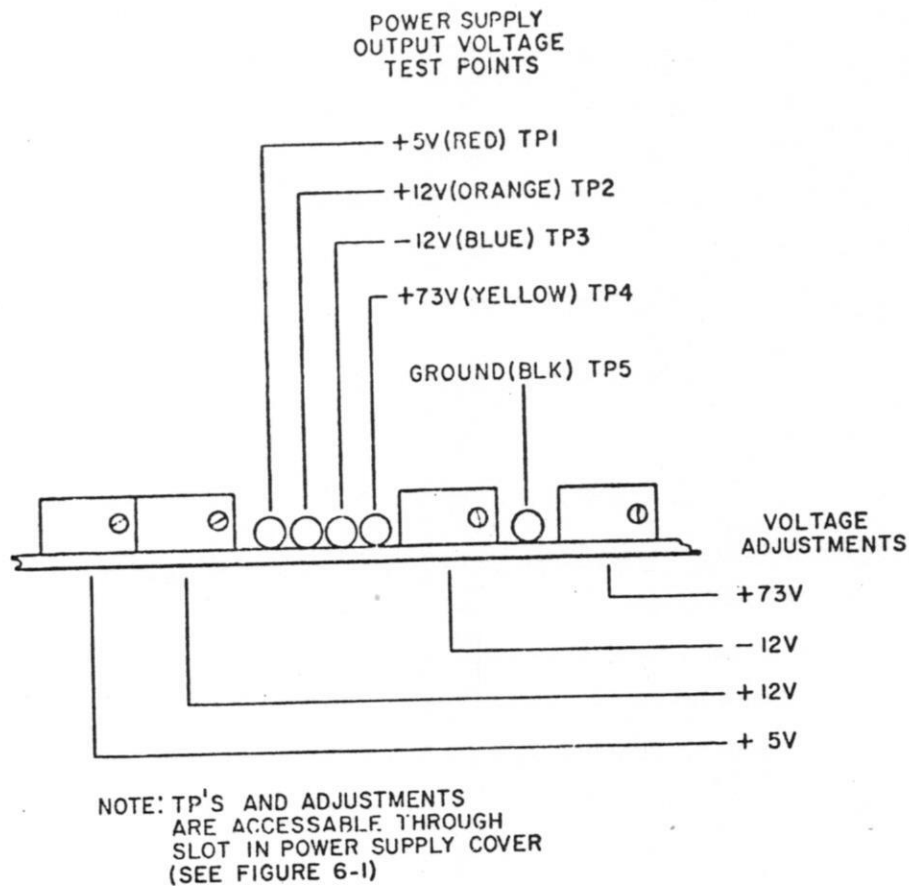


Figure 6-2. Power Supply Voltage Adjustments

- Set multimeter to read +12v.
- Adjust +12v potentiometer until multimeter indicates +12v.
- Remove test lead from orange test jack and connect it to red test jack (see Figure 6-2).
- Set multimeter to read +5v.
- Adjust +5v potentiometer until multimeter indicates +5v.
- Remove test lead from red test jack.
- Set multimeter to read -12v.
- Connect positive test lead of multimeter to blue test jack (see Figure 6-2).
- Adjust -12v potentiometer until multimeter indicates -12v.
- Remove test leads from printed-circuit board of power supply.
- Remove power from power supply.

TV MODULE ADJUSTMENTS.

The TV module (Figure 6-3) contains several display raster adjustments which are accessible with the cabinet hood removed. Depending on the time available for repair and the particular problem, the serviceman may adjust these circuits instead of removing and replacing the TV module. The following paragraphs describe those TV module adjustments which may be performed on-site. Table 6-1 summarizes each adjustment and references applicable incorrect adjustment identification figures. Figure 6-4 locates each adjustment described. Any adjustments not described in the following paragraphs are not intended for on-site use.

WARNING

DANGEROUS HIGH VOLTAGE EXISTS WITHIN THE CIRCUITS OF THE UNIT WHEN POWER IS APPLIED. USE EXTREME CAUTION WHEN MAKING ADJUSTMENTS. EVEN WITH POWER TURNED OFF AND/OR POWER CABLE REMOVED, CAPACITORS USED IN THE HIGH VOLTAGE VIDEO MODULE RETAIN CHARGE FOR SOME TIME AFTER POWER REMOVAL. BEFORE BEGINNING ANY ADJUSTMENTS, SEE AND FOLLOW COMPLETE SAFETY WARNING PROVIDED ON PAGE 6-8.

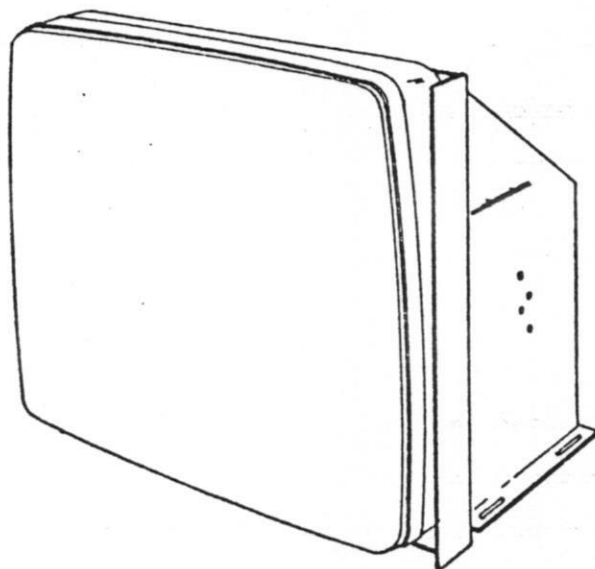


Figure 6-3. TV Module

TABLE 6-1. TV-MODULE ADJUSTMENT CONTROLS

ADJUSTMENT CONTROL	PURPOSE	TYPE	FIGURE NO. SHOWING INCORRECT ADJUSTMENT
Contrast	Adjusts degree of difference between black and white areas on display screen.	Potentiometer	6-6, 6-7
Vertical Hold	Prevents display from rolling vertically.	Potentiometer	6-8, 6-9
Horizontal Hold	Prevents display from tearing horizontally.	Potentiometer	6-10
Focus	Gives sharp, clear formations of letters.	Potentiometer	6-11
Vertical Size	Determines height of display.	Potentiometer	6-12
Vertical Linearity	Provides uniform height of all display lines	Potentiometer	6-13
Yoke	Rotates display clockwise or counterclockwise.	Magnetic Deflection Coil	6-14
Raster Centering	Moves display left-right or up-down.	Magnets	6-15

NOTE: Use a full display of letter "H"'s for visual inspection when performing adjustments (see Figure 6-5).

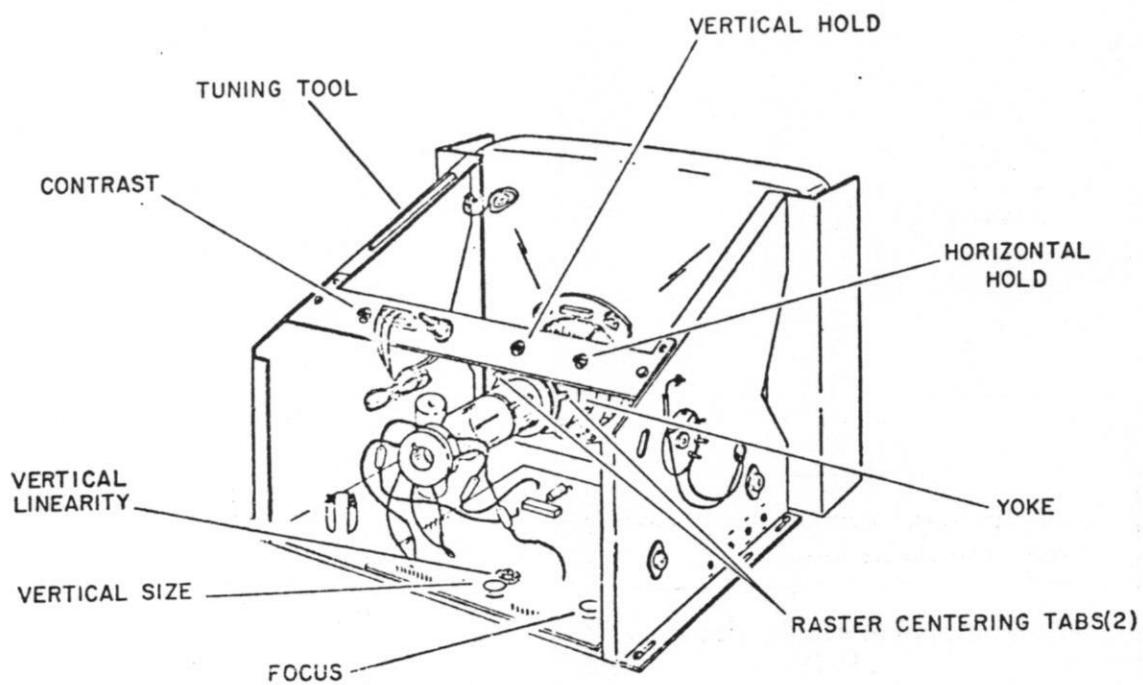


Figure 6-4. TV Module Adjustment Locations

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that the technician automatically takes precautions.
2. A GOOD PRACTICE, when working on any unit, is to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.
3. Extreme care should be used in HANDLING THE PICTURE TUBE as ROUGH handling may cause it to IMplode due to atmospheric pressure (14.7 lbs. per sq. in). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, use safety goggles and heavy gloves for protection. When removing the TV module or working on adjacent assemblies, ALWAYS DISCHARGE picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode using a well insulated piece of wire.
4. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on unit.

CONTRAST.

To adjust the contrast, perform the following:

- Turn Contrast control (slot head adjustment screw) fully counterclockwise (minimum contrast).
- Turn BRIGHTNESS control clockwise until raster is just visible.
- Turn Contrast control clockwise while at the same time turn BRIGHTNESS control counterclockwise until H's are clear and distinct.
- Continue rotating controls until Contrast control makes dots of H's begin to bloom (defocus).

- Turn Contrast control counterclockwise until dots are again sharp and clear.
- Adjust BRIGHTNESS control for desired brightness of display. (TO PROLONG LIFE OF CRT, BRIGHTNESS OF DISPLAY SHOULD NOT BE SET HIGHER THAN NECESSARY).

VERTICAL HOLD.

Adjust Vertical Hold control (slot head adjustment screw) until display does not roll or slip frames in vertical direction.

To adjust Vertical Hold control, perform the following:

- Turn Vertical Hold control clockwise until display begins to slip or roll vertically and note setting of control.
- Turn Vertical Hold control counterclockwise until display begins to slip or roll vertically and note setting of control.
- Set Vertical Hold control to midpoint of two settings noted in previous steps.

HORIZONTAL HOLD.

Adjust Horizontal Hold control (slot head adjustment screw) until display does not warp diagonally.

To adjust the Horizontal Hold control, perform the following:

- Turn Horizontal Hold control clockwise until display begins to tear horizontally and note setting of control.
- Turn Horizontal Hold control counterclockwise until display begins to tear horizontally and note setting of control.
- Set Horizontal Hold control to midpoint of two settings noted in previous steps.

FOCUS.

Adjust focus control (slot head adjustment screw) until dots composing all H's in display are sharp and clear.

VERTICAL SIZE.

Adjust Vertical Size control (cross head adjustment screw) for display height of 4.9 ± 0.3 in. (12.4 ± 0.8 cm).

VERTICAL LINEARITY.

Adjust Vertical Linearity control (slot head adjustment screw) for equal height of H's in all display lines (control has greatest effect upon top and bottom lines).

YOKE.

To rotate raster clockwise or counterclockwise, perform the following:

- Loosen nut on yoke clamp on neck of CRT.
- Rotate yoke in direction necessary to place raster in level position (no tilt).
- Tighten nut carefully on yoke clamp so yoke is held firmly to CRT neck.

RASTER CENTERING.

Adjust raster left-right or up-down by moving the two Raster Centering tabs on neck of CRT. Readjust focus, if necessary, after completing raster positioning.

REMOVE AND REPLACE PROCEDURES.

WARNING

To prevent personal injury or equipment damage resulting from electrical shock, the following three steps must always be followed when removing or replacing assemblies or subassemblies of the display station.

- Depress POWER indicator/switch. POWER indicator extinguishes.
- Remove display station AC power cord from site AC power outlet.
- Clear all unnecessary equipment from work area.

CABINET HOOD.

To remove the cabinet hood, perform the following:

- Verify display station AC power cord is removed from site power outlet.
- Disconnect communications cable connectors from connector panel.
- Loosen two mounting screws located at lower back corners of cabinet hood (see Figure 6-16).
- Grasp both sides of hood and carefully slide it back toward rear of display station until hood clears framework.

To replace the cabinet hood, reverse the preceding procedure making certain that the holding tabs (two on each side), on the inner side of the front side panels, engage the keyboard mounting bracket. Also, the power plug interlock at the rear of the hood, must be seated firmly with the mating connector on the terminal chassis.

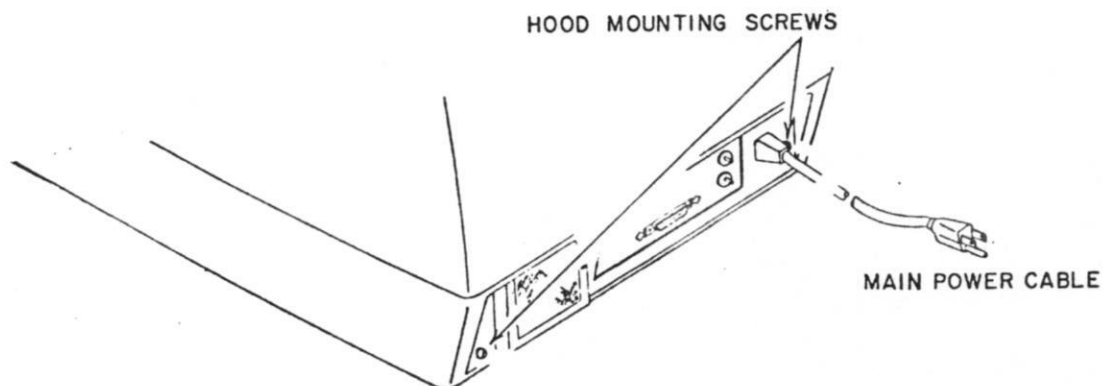


Figure 6-16. Cabinet Hood Mounting

POWER SUPPLY MODULE.

To remove the power supply module, perform the following:

WARNING

When removing or replacing the power supply module, DO NOT STRIKE THE NECK OF THE CRT with the power supply. The extremely high vacuum of the CRT can cause it to implode producing serious injury. Safety goggles should be worn.

- Verify display station AC power cord is removed from site power outlet.
- Refer to cabinet hood removal and remove cabinet hood.
- Place identifying tags on each cable to power supply so that each cable may be later reconnected to its correct connector.
- Disconnect all cables from power supply module (see Figure 6-17).
- Remove two mounting screws from mounting tabs located at rear of power supply module (see Figure 6-17).
- Grasp power supply on each side and gently slide it toward rear of display station until two front holddown tabs are free of holddown tab slots in main chassis.

To replace the power supply module, reverse the preceding procedure.

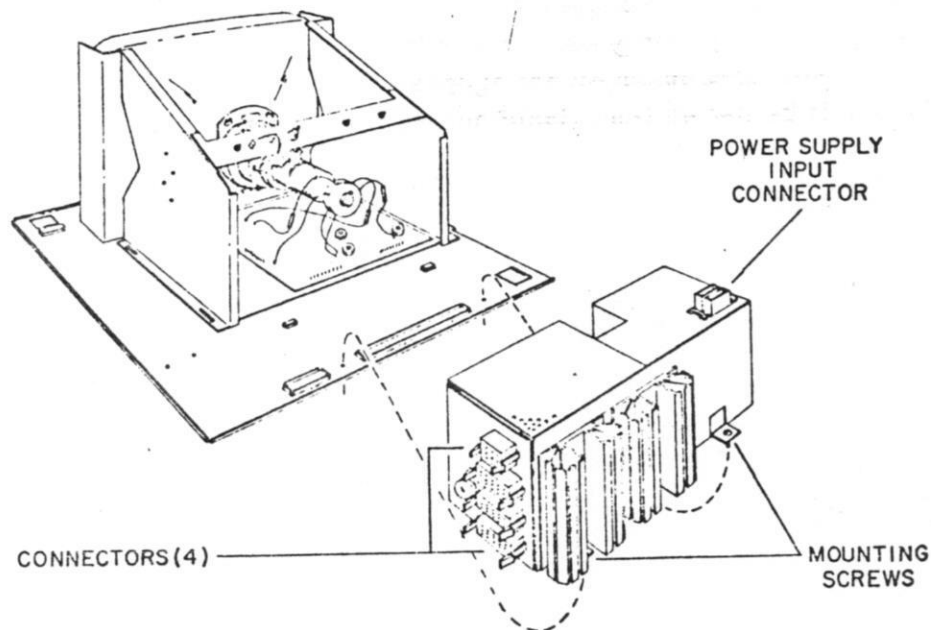


Figure 6-17. Power Supply Module Mounting

LOGIC MODULE.

To remove the logic module, perform the following:

- Verify display station AC power cord is removed from site power outlet.
- Refer to cabinet hood removal and remove cabinet hood.
- Place identifying tags on each external cable to logic module so that each cable may be later reconnected to its correct connector.
- Disconnect all external cables from logic module (see Figure 6-18). Do not disconnect inter-board cable connectors.
- Remove two mounting screws, located at rear of logic module, from mounting tabs (see Figure 6-18).
- Slide logic module carefully toward rear of display station until from holddown tab is free of holddown tab slot in main chassis.
- Lift logic module clear of display station.

To replace the logic module, reverse the preceding procedure.

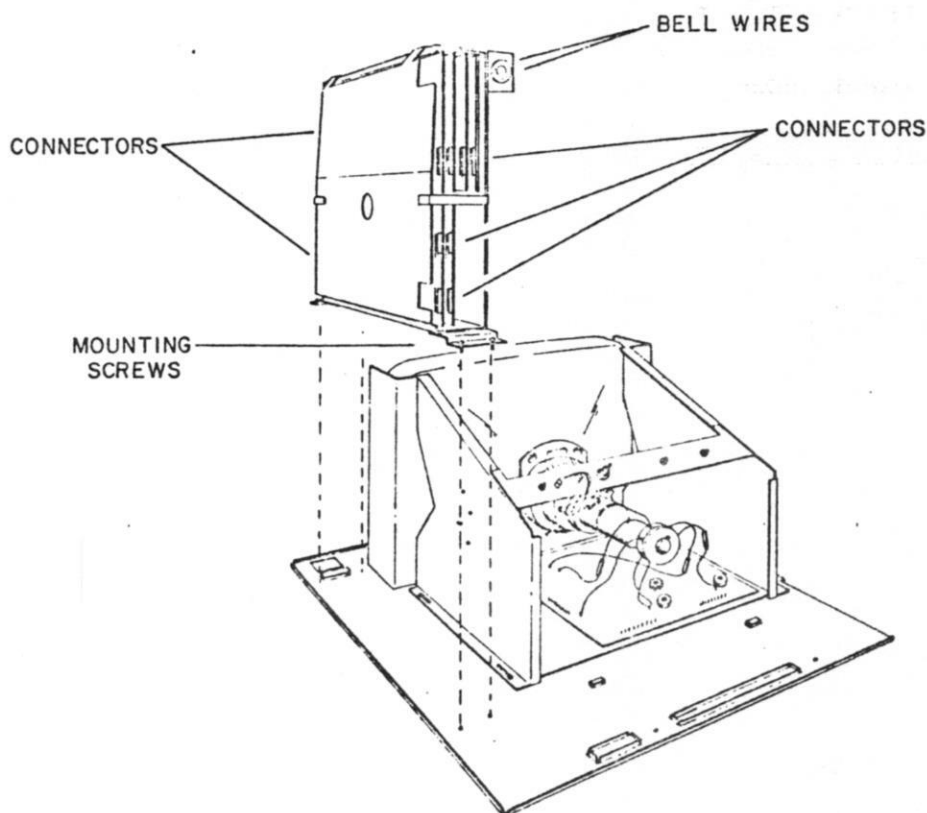


Figure 6-18. Logic Module Mounting

TV MODULE.

To remove the TV module, perform the following:

WARNING

Use extreme care when HANDLING THE TV MODULE as rough handling may cause the CRT to implode causing severe injury. Do not nick or scratch glass or subject it to any undue pressure during removal or replacement. When handling, use safety goggles and heavy gloves for protection.

- Verify display station AC power cord is removed from site power outlet.
- Refer to cabinet hood removal and remove cabinet hood.

WARNING

Discharge picture tube by shorting the anode connection to chassis ground. Use a well insulated piece of wire.

- Refer to display power supply removal and remove power supply.
- Disconnect all cables from TV module (see Figure 6-19).
- Remove four mounting screws (see Figure 6-19).
- Grasp TV module on each side of its frame and carefully lift it clear of display station.

To replace the TV module, reverse the preceding procedure. Insure that the insulating washers between the TV module frame and mounting plate (one at each screw location) are replaced. If necessary, readjust focus after replacing TV module.

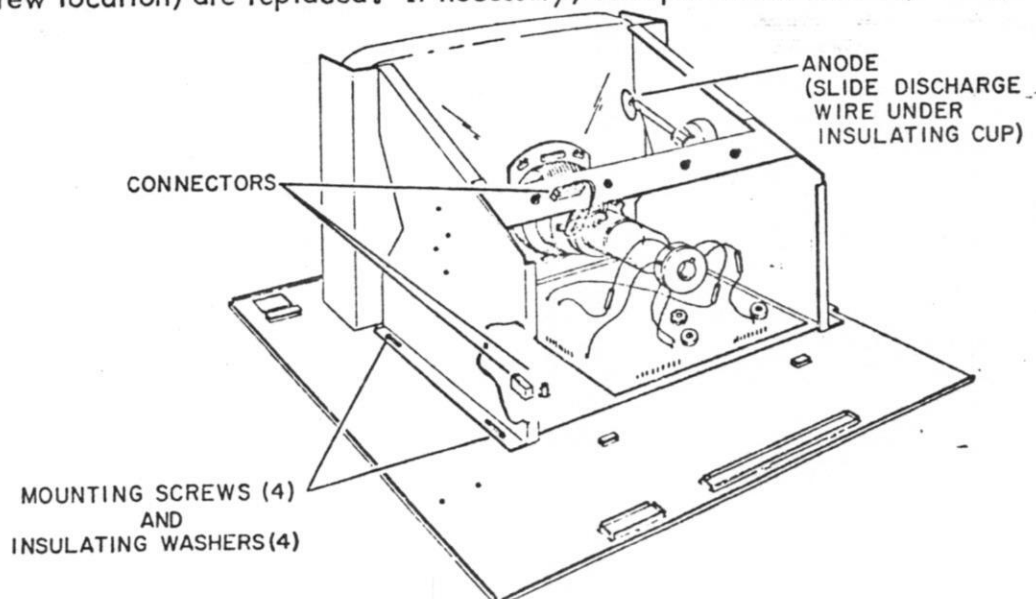


Figure 6-19. TV Module Mounting

KEYBOARD MODULE.

To remove the keyboard module, perform the following:

- Verify display station AC power cord is removed from site power outlet.
- Refer to cabinet hood removal and remove cabinet hood.
- Remove power supply input connector and feed cable through cutout in mounting plate (see Figure 6-17).
- Remove two keyboard-tray holding screws located beneath front edge of keyboard.
- Grasp keyboard on both sides and slide it forward until two mounting screws, located beneath rear corners of keyboard, are accessible.
- Disconnect cables from keyboard module (see Figure 6-20).
- Remove three mounting screws located beneath keyboard (one is located at front center of keyboard, and two are located at rear corners).
- Slide keyboard back in its mounting channel until front holddown tabs are free of holddown slots in channel frame.
- Lift keyboard free of display station.

To replace the keyboard module, reverse the preceding procedure.

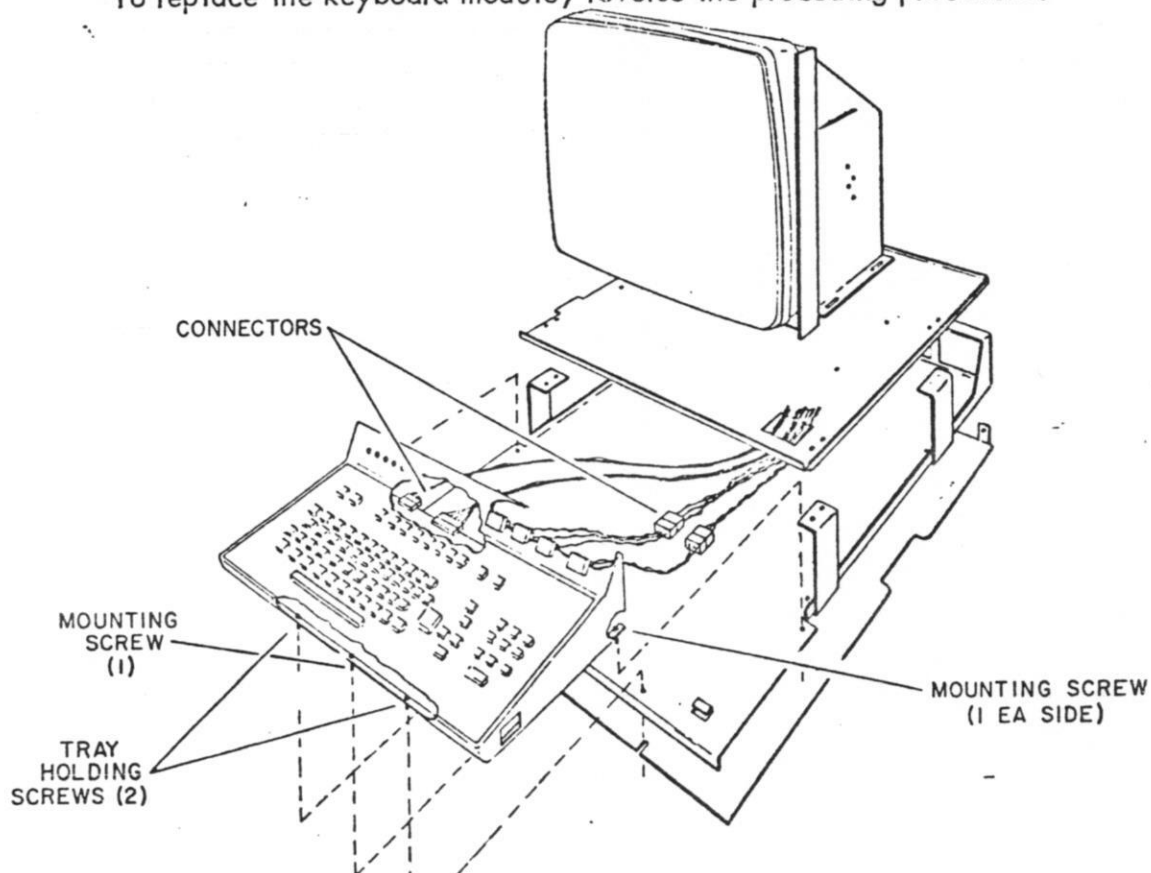


Figure 6-20. Keyboard Module Mounting

DISPLAY FACEPLATE.

To remove the display faceplate, perform the following:

- Verify display station AC power cord is removed from site power outlet.
- Refer to cabinet hood removal and remove cabinet hood.
- Remove screw holding BRIGHTNESS control knob and remove knob.
- Remove KEYLOCK key.
- Remove two screws attaching Keylock assembly to viewing screen.
- Remove two viewing screen mounting screws located beneath front edge of plate which display faceplate mounts on.
- Grasp viewing screen on both sides and gently slide forward until hold-down tabs along front edge disengage from mounting plate, then, lift it free.

To replace the display viewing screen, reverse the preceding procedure.

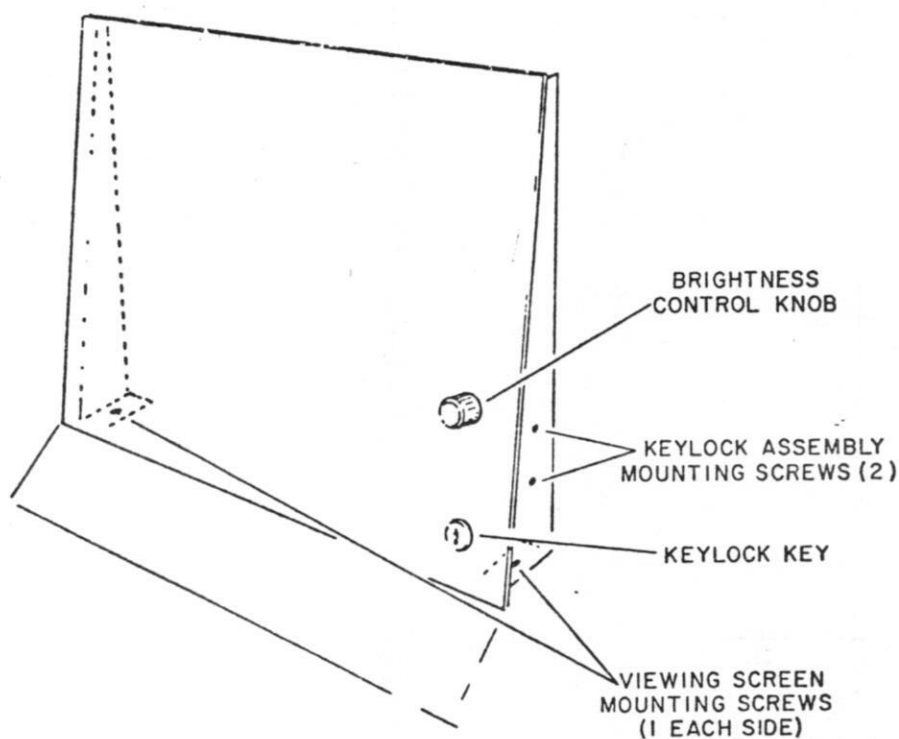


Figure 6-21. Display Faceplate Mounting

MISCELLANEOUS FIELD SPARE PARTS.

When removing or replacing field spare parts not described thus far, refer to the diagrams of Section VII for parts location. Refer to "Cabinet Hood" for removal instructions to gain access to the inside of the display station. ALWAYS MAKE CERTAIN DISPLAY STATION AC POWER CORD IS REMOVED FROM SITE POWER OUTLET BEFORE WORKING INSIDE UNIT.

SECTION VII

SPARE PARTS CATALOG

This section provides parts information necessary for on-site repair of Conversational Display Terminals by qualified technical personnel. Three types of parts documentation are included herein, 1) Genealogy Charts, 2) Spare Parts Lists, and 3) Assemblies with their parts lists down to the level of interest for on-site maintenance.

GENEALOGY CHARTS.

The included genealogy chart shows the relationship of assemblies and sub-assemblies for the terminal.

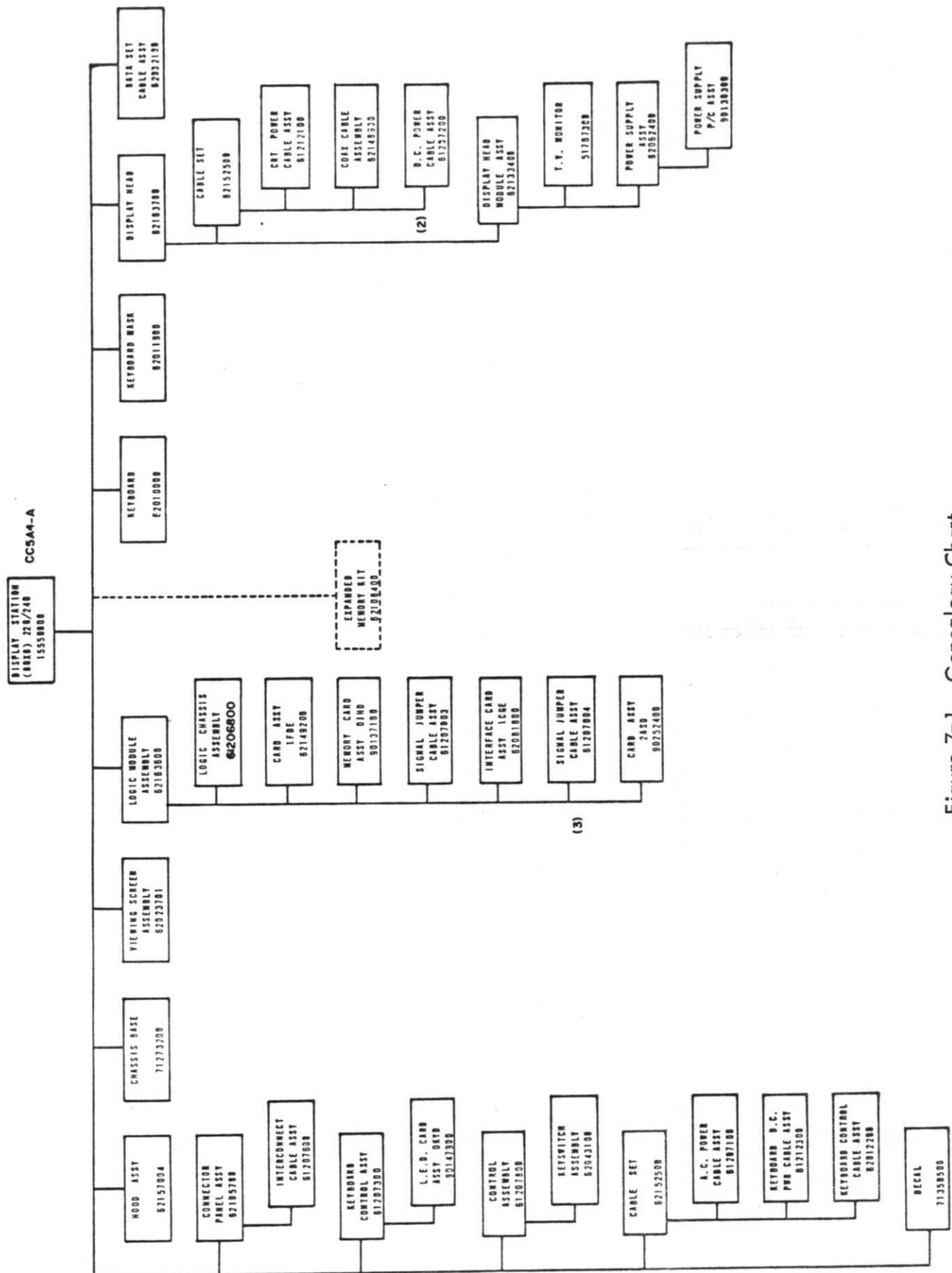


Figure 7-1. Genealogy Chart

SPARE PARTS LISTS.

Documents SPL 65932700 and SPL 65932800 are the spares lists for the terminal.

CIT

Spare Part Kit #2

50

Display Terminal, (1/2)

SPL

65932800

FIRST USED ON

CC 5A4-A

CODE IDENT
15920

SHEET

OF 2

REVISION RECORD

SHEET REVISION STATUS

REV	DATE	DESCRIPTION	BY	CHKD
1				
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6				
7				
8				
9				
10				
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NOTES:

65932800

DETACHED LISTS

PRINTED IN U.S.A.

Part of 2
Medium Display Terminal)

COD. GEN.

15920

SHEET

2 of 2

SPL

LOW

NO

65932800

SPECIFICATION
NOTES, OR MATERIAL

NOMENCLATURE
OR DESCRIPTION

UNIT
OF
MEAS.

QUANTITY REQUIRED

UNIT

62163600

62163600

62010000

62010000

62010000

62010000

Logic Module Assembly

Keyboard Assembly

TV Monitor

Power Supply Assy

2

2

2

2

1

CIT

Spare Part File #1

50

NUM Display Terminal, X 10

FORM 100-10

CC 5A4-A

NUM

CODE IDENT

15-20

65932700

CHARTER

SPL

HEET

100-10

SHEET REVISION STATUS

REVISION RECORD

4 3 2 1

CCO

STATION

DATE

NOTES:

- 1. EQUIPMENT CONFIGURATOR 15550700
- 2. TOP LEVEL ASSEMBLY 15550800
- 3. ON-SITE SPARE PARTS 65932800

APL 65932700

DETACHED LISTS

CODE IDENT
 15920

SHEET 2 of 4

SPL

65932700
mm

SPECIFICATIONS,
 NOTES, OR MATERIAL

ITEM NO	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	51338900 <i>mm</i>											PC	Can <i>mm</i>	
2	62013040											PL	Radio Alarm	
3	62010240											PC	Switch (power on)	
4	62011200											PC	Switch	
5	62012500											PC	Lens (scroll display)	
6	62012505											PC	Lens (printer on line)	
7	62012544											PC	Lens (local)	
8	62012546											PC	Lamp Incandescent	
9	25113006											PC	Card Assembly (870)	
10	62012700											PC	Connector 15 pin of AS	
11	62013001											PC	Connector 25 pin of AS	
12	62013002											PC	Contact Switch 25 pin of AS	
13	62013002											PC	Contact Switch 25 pin of AS	
14	25113002											PC	Connector 35 pin	
15	62013006											PC	Contact 1 pin Plug	
16	62017600											PC	Light Emitting Diode	
17	62013100											PC	Switch-Key Lock	
18	62011115											PC	Circuit Breaker	
19	62013070											PC	Switch Relay	
20	62013070											PC	Switch	

Part 4 of 4 (Core Part Kit of Display Terminal)

CODE IDENT
15926

SHEET
3 of 4

SPL

DOCUMENT NO
45932700
Wm

LINE NO	PART IDENTIFICATION	QUANTITY REQUIRED					UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
21	6149240	2					pc	Switch slide 413	
22	6201240	2					pc	Connector lever	
23	6002140	5					pc	Contact, PTH	
24	6155707	2					pc	Connector 13 pin 14142	
25	6306340	2					pc	Contact slider 18123	
26	6202150	2					pc	Contact socket 12-2422	
27	6006300	5					pc	Filter-Vin Washable	
28	600211X	2					pc	Card-IO outlet	
29	6107180	2					pc	IC 171 (Quad 2 Input) (9202)	
30	6171180	5					pc	IC 171 Hex 4pin (9215)	
31	625340	2					pc	IC 1 of 12 Decoder	
32	6175100	2					pc	IC TTL 2 bit 20pin (9212)	
33	61758300	2					pc	IC 1094 14pin 14pin Quad 20	
34	61701900	2					pc	IC 1001 Dual 2 Input (9205)	
35	61771600	2					pc	IC 1001 Dual 2 Input	
36	6175470	2					pc	IC 1001 Dual 2 Input	
37	62021700	5					pc	IC TTL 4 pin 4pin Reg (9206)	
38	61752400	5					pc	IC TTL 14pin 2 Input 6.4 (9204)	
39	62051900	2					pc	IC TTL 8 Input Gate (9207)	
40	62051900	5					pc	Integrated CKT	

Compare Part Kit #1
(Display Terminal)

CODE IDENT

15920

SHEET

4 of 4

SPL

DOCUMENT NO

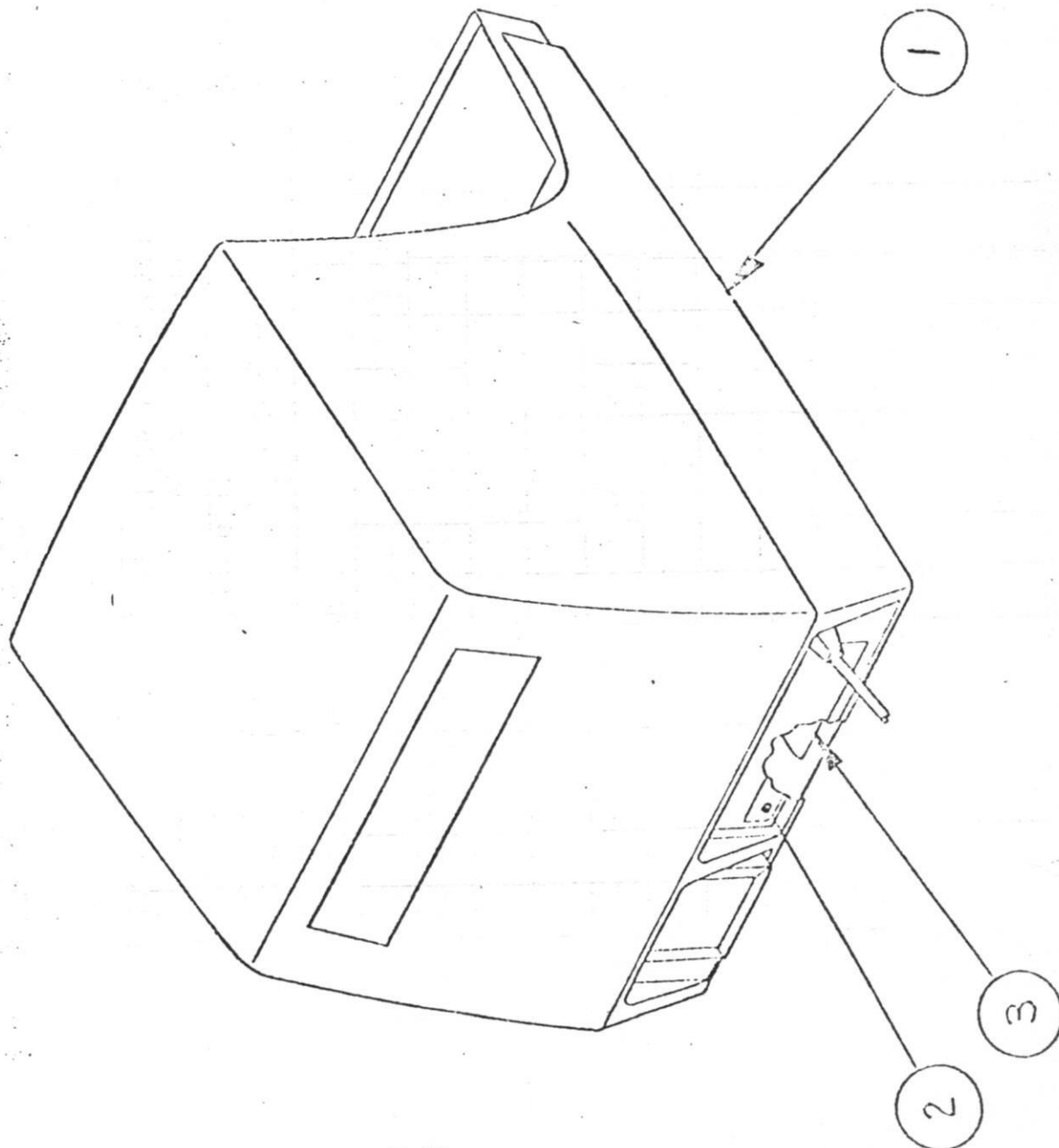
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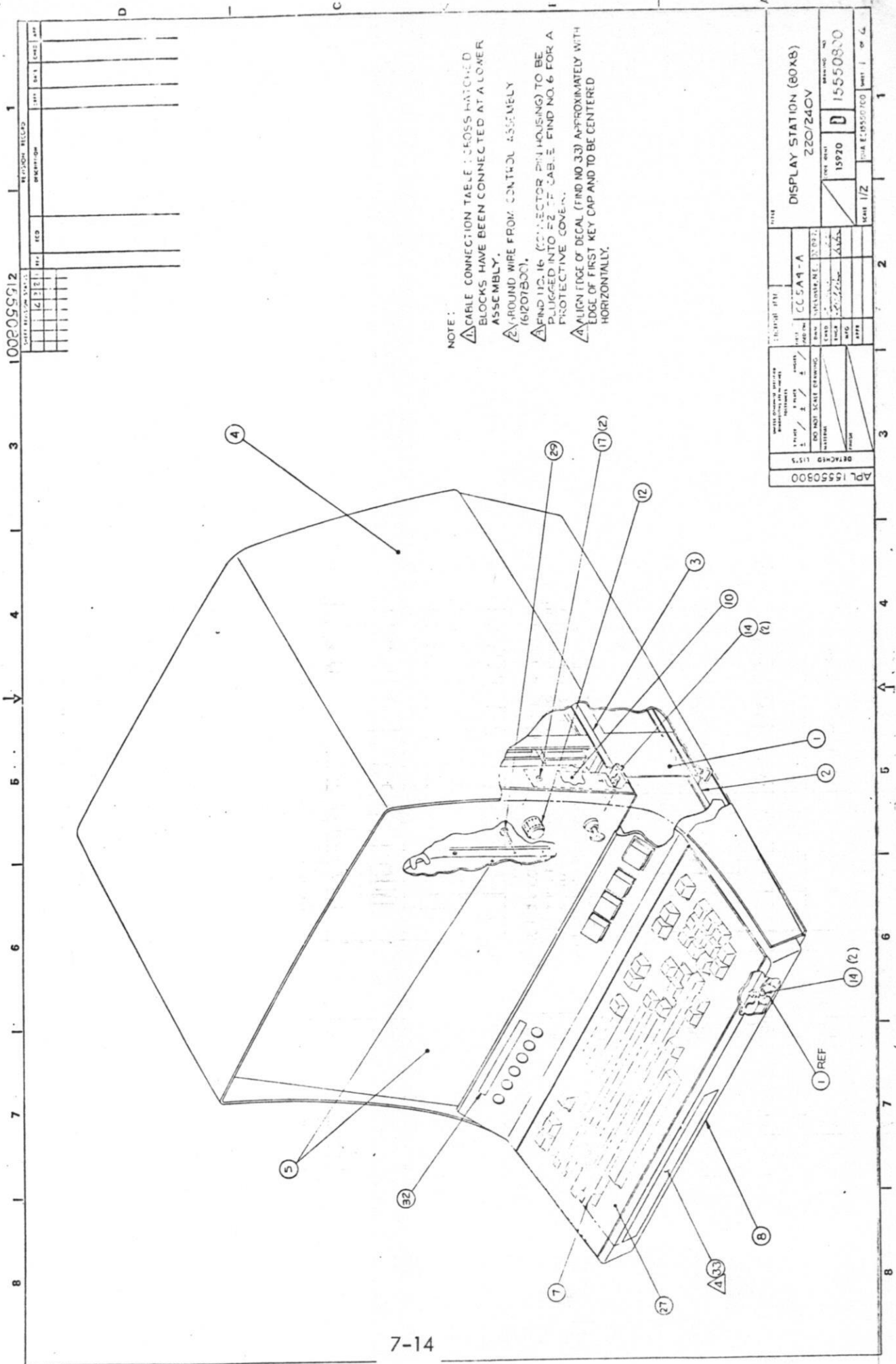
P/N	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
41	51761500	8										PC	IC TTL 4 Bit Flip-Flop (9014)	
42	51761800	2										PC	IC Quad Exclusive-OR Gate (9014)	
43	36183600	2										PC	IC TTL 4 Bit 2-Input OR Gate	
44	51761700	2										PC	IC Dual Line Receiver (71107)	
45	51761400	2										PC	IC TTL (9011)	
46	51761700	2										PC	IC Dual Line Driver (75110)	
47	51767304	2										PC	Printed CRT Board	
48	51767307	2										PC	Vertical Output Amplifier	
49	51767306	2										PC	Vert Output Transistor	
50	51767307	2										PC	Silicon VV Rectifier	
51	51767308	2										PC	Resistor Block	
52	51767309	2										PC	Flyback Transformer	
53	51767310	2										PC	Reflection Tube	
54	51767302	2										PC	CRT VFO Face Panel	
55	36180500	2										PC	IC MC1489	
56	36180500	2										PC	IC MC1489	
57	36180501	2										PC	Connector, 9 Pin Housing	

ASSEMBLIES.

Assembly drawings with accompanying parts lists provide parts data to a level required for on-site equipment maintenance. The remainder of this section contains such applicable assembly documentation as available at the time of this manual's preparation.

RE	DOC. INTA	15550700	A	SHEET 2	CODE IDENT 15920	DISPLAY STATION 50x5 220/24V
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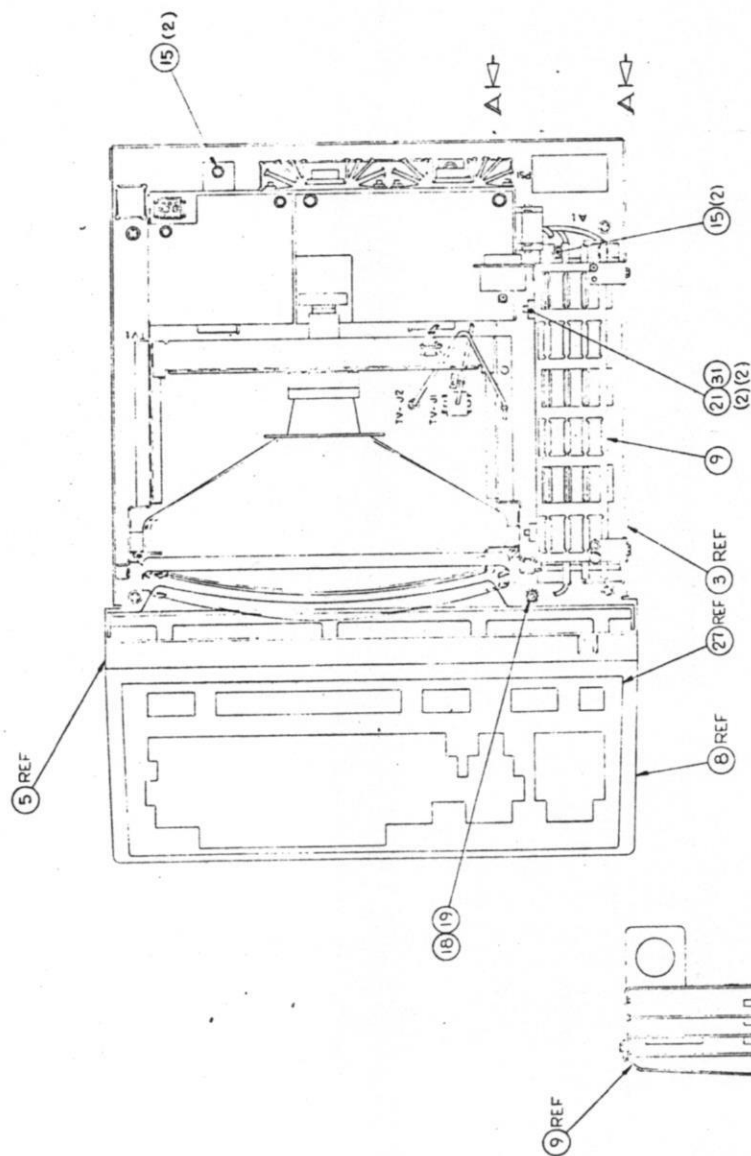




NOTE:

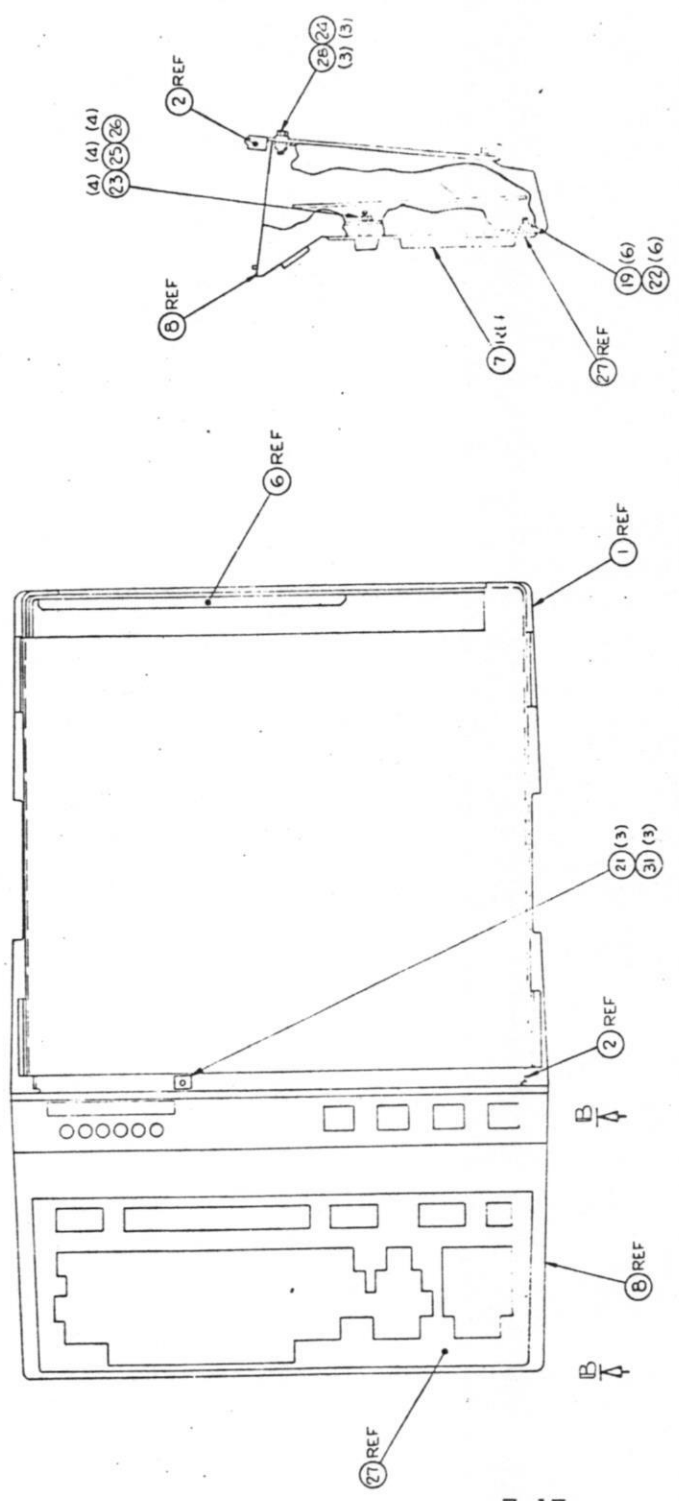
- △ CABLE CONNECTION TABLE: CROSS-HATCHED BLOCKS HAVE BEEN CONNECTED AT A LOWER ASSEMBLY.
- △ AROUND WIRE FROM CONTROL ASSEMBLY (62078300).
- △ FIND 12-16 (COLLECTOR PIN HOUSING) TO BE PLUGGED INTO P2 OF CABLE FIND NO. 6 FOR A PROTECTIVE COVER.
- △ ALIGN EDGE OF DECAL (FIND NO. 33) APPROXIMATELY WITH EDGE OF FIRST KEY CAP AND TO BE CENTERED HORIZONTALLY.

APL 15550900		DRAWING 1155	
DO NOT SCALE DRAWING		SCALE 1/2	
DATE 15550900		DATE 15550900	
BY 15550900		BY 15550900	
CHKD 15550900		CHKD 15550900	
APPD 15550900		APPD 15550900	
CCL 5A4-A		CCL 5A4-A	
220/240V		220/240V	
DISPLAY STATION (80x8)		DISPLAY STATION (80x8)	



TOP VIEW
HOOD (ITEM 4) REMOVED FOR CLARITY

REV	ECO	REVISION	REVISION	DATE	BY	CHKD	APP
1		100805951					



VIEW B-B
(ROTATED 90° CCW)

TOP VIEW
ITEMS 3 & 4 REMOVED FOR CLARITY

REV	ECO	REVISION	REVISION	DATE	BY	CHKD	APP
1		100805951					

DISPLAY STATION (80x8)
220/240 V

15920 D 15550300

15920 D 15550300

ITEM NO.	STATUS DATE	FROM STATUS	TO STATUS	ENG. RESP.	DWG. SIZE	DESCRIPTION	ECO. NO. & REV.	SERIAL NO.	EFF. DATE
02	03-72	37-39	40-42	43-50	51	D DISPLAY STATION 80x8 220/240V	44-45	54-58	59-63
TRANSACTION CODES:									
1. DELETE LINE ITEM(S) WITH HISTORY									
2. DELETE ASSY P/L FROM FILE									
3. ADD ASSY P/L TO FILE									
4. DELETE LINE ITEM(S) WITH NO HISTORY									
5. CHANGE, ADD, OR DELETE ANY FIELD EXCEPT "ECO OUT" & "WK OUT" OR CURRENT RECORD									
6. CHANGE, ADD, OR DELETE ANY FIELD EXCEPT "ECO IN" & "WK IN" OR CURRENT RECORD.									
7. REQUEST PARTS LIST ONLY									
8. CHANGE, ADD, OR DELETE ANY FIELD EXCEPT "ECO IN" & "WK IN" OR CURRENT RECORD.									
9. ADD LINE ITEM(S)									
2	1	711273300				BASE TERMINAL			
2	2	711273200				CHASSIS - BASE			
2	3	62163700				DISPLAY HEAD			
2	4	62157000				HOOD ASSEMBLY 240V			
2	5	62023701				PANEL ASSEMBLY VIEWING			
2	6	62105700				CONNECTOR PANEL ASSEMBLY			
2	7	62010000				KEYBOARD			
2	8	61207300				KEYBOARD CONTROL ASSEMBLY			
2	9	62163600				LOGIC MODULE ASSEMBLY			
2	10	61207800				CONTROL ASSEMBLY			
2	11	62137500				CABLE SET			

STATUS DATE	FROM STATUS	TO STATUS	ENG. RESP.	DWG. SIZE	DESCRIPTION	PREPARED BY	DATE
31-36	37-39	40-42	43-50	51	52-80	W.E. Watkins	02-04-72
02-04-72				D	DISALAY STAT, 10M 80x8	AUDITED BY	DATE
						W.E. Watkins	02-04-72

COIL	36	101
1-2	3	4
ASSEMBLY NUMBER	7-16	
DIG.	17	18-19
REV.		

TRANSACTION CODES:

1. DELETE ASSY P/L FROM FILE
2. ADD ASSY P/L TO FILE
3. DELETE LINE ITEM(S) WITH NO HISTORY
4. ADD LINE ITEM(S)
5. DELETE LINE ITEM(S) WITH HISTORY
6. CHANGE, ADD, OR DELETE ANY FIELD EXCEPT "ECO OUT" & "WK OUT" OR CURRENT RECORD
7. REQUISIT PARTS LIST ONLY
8. CHANGE, ADD, OR DELETE ANY FIELD EXCEPT "ECO IN" & "WK IN" OR CURRENT RECORD

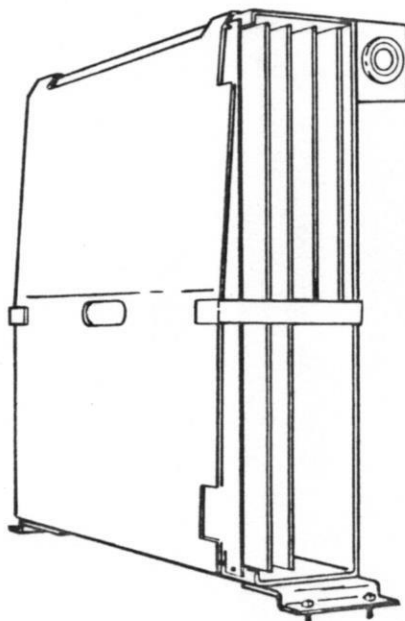
FIND NO.		L.N.		PART NUMBER		QTY		QUANTITY		DESCRIPTION		ECO. NO. & REV.		SERIAL NO.		REF. NO.	
20 - 22		23 - 24		25 - 34		35 - 36		37 - 43		(REF. ONLY)		44 - 53		54 - 58		59 - 63	
2	34			62154400				1			AC POWER CABLE ASSY						
2	35			65932390				REF			SPARE PART KIT No 1						
2	36			65932800				REF			SPARE PART KIT No 2						
2	37							REF			WIRING DIAGRAM - POWER DIST						
2	38			59109100				REF			PACKAGING INSTRUCTIONS						



CONTROL DATA[®]

DISPLAY LOGIC MODULE

Part No. 62163600



CONTROL DATA
CORPORATION

**REPAIR CENTER
CUSTOMER ENGINEERING MANUAL**

DISPLAY LOGIC MODULE
PART NO. 62163600

Publication No.
62990800

Address comments concerning
this manual to:

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A

FOREWORD

This repair center customer engineering manual provides technical information to aid in repairing the display logic module, part no. 62163600. It includes maintenance information for the basic logic module which contains circuit cards as follows.

<u>Card Type</u>	<u>Card Function</u>	<u>Card Assembly</u>
1FDE	Basic Control	62149300 (Qty 1)
1CGE	Interface	62081800 (Qty 1)
2ASD	Interface	90252400 (Qty 1)
0JHD	Memory	90137100 (Qty 1)

This manual contains eight sections. Section 1 provides a general description of the logic module. Section 2 describes the controls, indicators, interface signals, input/output functions, and the programming procedures. Section 3 references the installation and checkout of the logic module. Section 4 provides a general discussion of the logic module operation. Section 5 provides logic diagrams to help understand the operation, maintenance, and troubleshooting of the logic module. Section 6 describes preventive and corrective maintenance. Section 7 provides information to aid in locating a fault in the operation of a logic module. Section 8 contains parts data.

In addition to the basic card types described in this manual, the logic module is designed to contain the following additional logic circuit cards:

<u>Card Type</u>	<u>Card Function</u>	<u>Card Assembly</u>	<u>Repair Center Manual Publication Number</u>
0JHD	Expanded Memory	90137100 (Qty 1)	62101900

For detailed repair center information covering these circuits, refer to the IAT Display Logic Module Circuit Cards, publication no. 62987900.

For similar information on associated equipment assemblies, refer to the specific repair center customer engineering manual for the specific assembly.

Additional copies of this manual may be ordered from:

Control Data Corporation
Literature and Distribution Services
8100 34th Avenue South, P.O. Box 0
Minneapolis, Minnesota 55440

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SECTION 1

GENERAL DESCRIPTION

This section provides a general description of the display logic module. The logic module is one of three modules involved with data handling within the display terminal. Logic module circuits provide routing and controlling of the data. The TV module provides display of the data, and the keyboard module provides means of operator input. Application of the logic module is shown in figure 1-1.

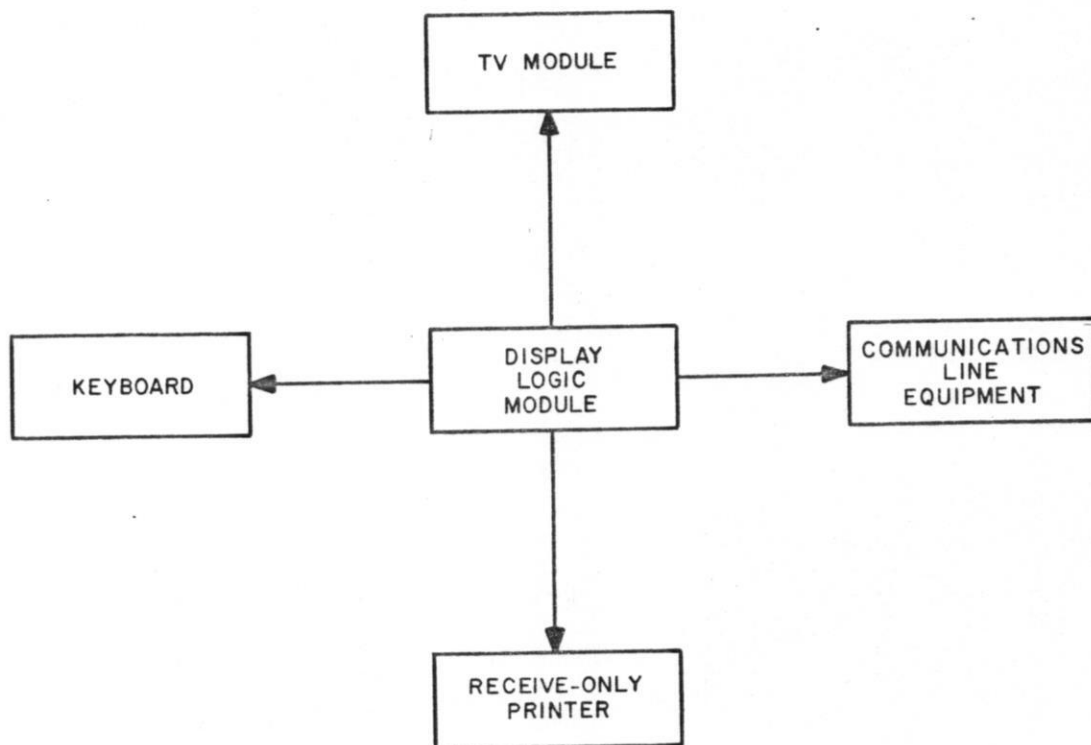


Figure 1-1. Typical Display Logic Module Application

TERMINAL CONFIGURATION

Data is entered into the terminal by the keyboard or the interface circuits, and is transmitted from the terminal to a printer via the printer interface circuits or to the modem via the transmit interface circuits. The control logic provides timing, sequence, and character generation circuits for the internal functions of the display terminal. Figure 1-2 shows the logical configuration of the display terminal.

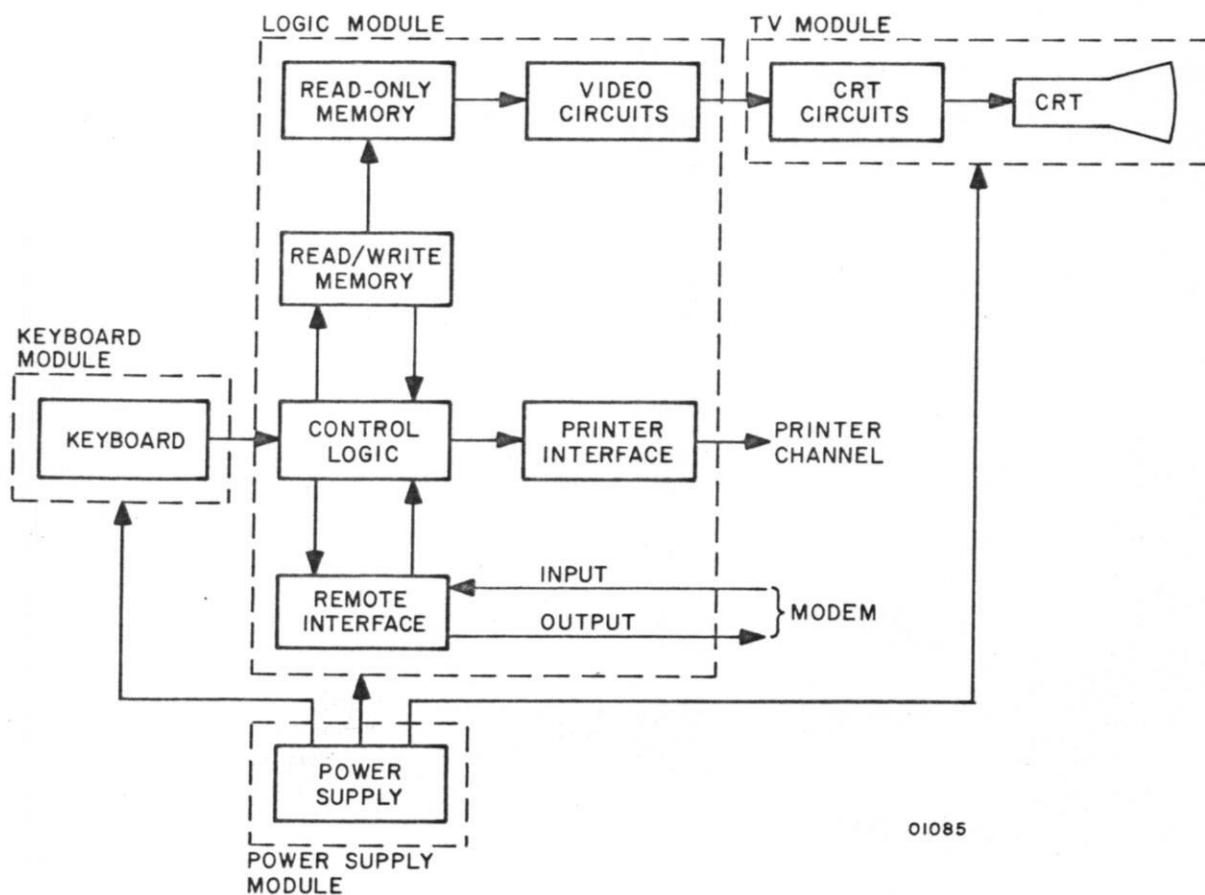


Figure 1-2. Display Terminal Configuration

The operator enters data when the keyboard is unlocked and no data is being received by the terminal. The read/write memory furnishes storage for the character codes which the logic module uses to refresh the CRT display or to transmit data to optional external printing equipment. Data read from the read/write memory is referenced by the read-only memory (ROM) to determine the character to be displayed. The preprogrammed ROM contains a character matrix which supplies the bits to build the video pulse train which unblanks the CRT electron beam to form the character matrix on the display screen in the TV module.

The interface circuits communicate at rates of 75, 110, 150, 200, and 300 serial bits of data per second. The interface circuits perform two functions, receive data and send data. Data originating from a remote device such as a processor is received by the terminal from the modem and routed through the receive interface circuits.

A receive data function commands the logic circuits to transfer any code on the receive data line into the read/write memory. As this information is received and stored in the read/write memory, it is also displayed as part of the refresh cycle. A send data sequence occurs when a keyboard strobe is received by the logic module and the module is not in a receive sequence or local mode.

The display terminal transmits data as it is entered at the keyboard. The circuits operate in either remote or local mode depending on the position of the LOCAL switch. Remote operating mode is used to transmit data between a terminal and remote equipment. Local mode disables the transmit interface and stores keyboard entered data in the read/write memory for display. Printer control circuits enable the display terminal to transmit to an associated printer via the printer interface circuits.

CIRCUIT CARD FUNCTIONS

The logic module contains four basic functional areas as shown in the block diagram of figure 1-3. These functions are contained on four circuit cards located in the logic module chassis shown in figure 1-4.

The circuit cards use integrated circuits to produce the necessary functions. The integrated circuits are Fairchild 9300 series commercial medium-scale integration (MSI), 9000 series commercial transistor-transistor logic (TTL), and differential amplifiers for interface drivers and receivers.

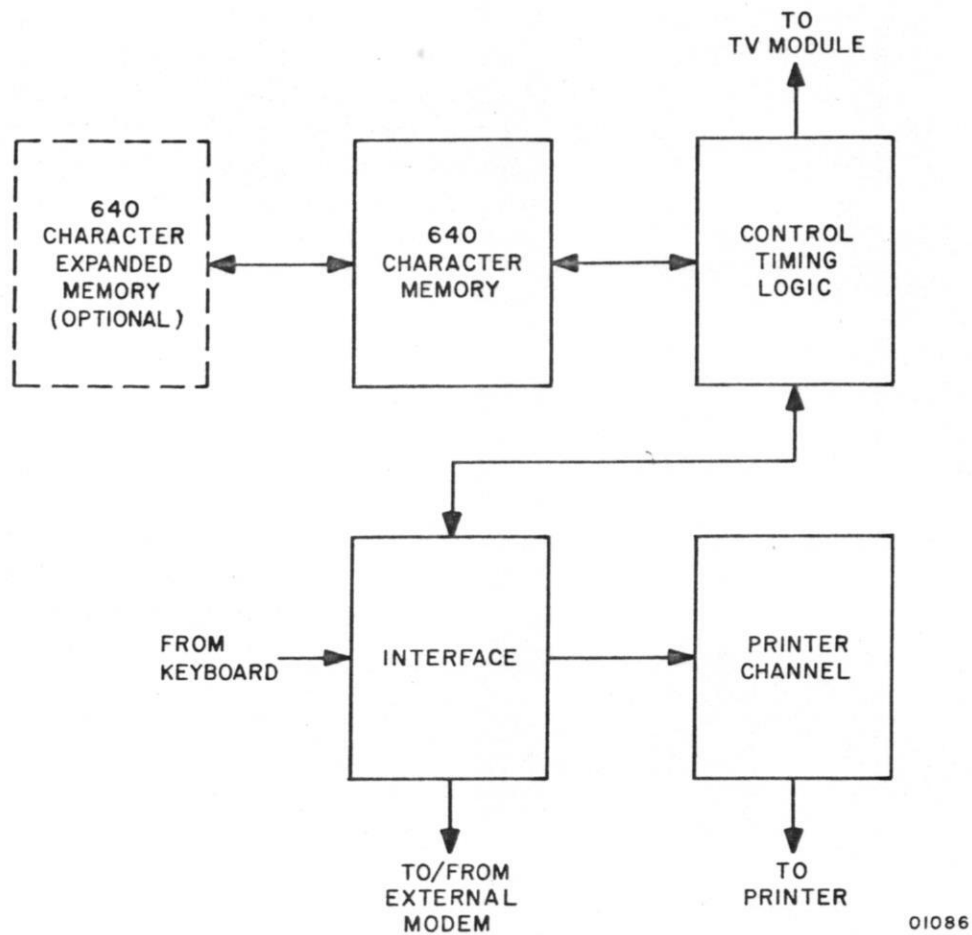


Figure 1-3. Display Logic Module Functional Block Diagram

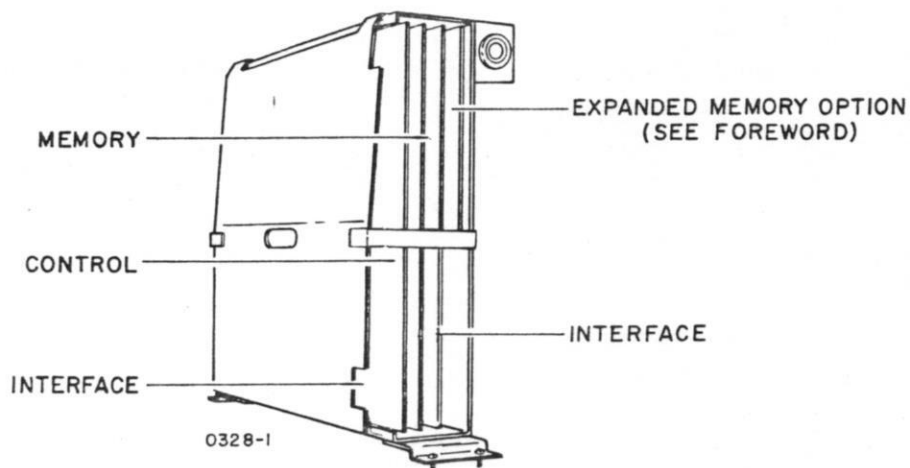


Figure 1-4. Logic Module with All Cards in Place

READ/WRITE MEMORY (640 CHARACTERS)

The read/write memory card uses large-scale integration (LSI), metal oxide semi-conductors (MOS) shift registers to store 640, 7-bit ASCII character codes for a display refresh. The printer channel also uses the character codes stored in the memory for a page print operation. The memory supplies a display refresh at 60 hertz. Memory access time is 63.6 microseconds. This basic memory provides for a display of 8 lines of 80 characters.

CONTROL LOGIC

The control logic provides timing, sequencing, and character generation circuits necessary for the internal functions of a terminal. A 20-MHz oscillator supplies the master timing for the control logic. The character generation circuit uses a large scale integrated (LSI) read-only memory (ROM) which supplies 96 standard ASCII character codes plus three special character codes. The ROM is a metal oxide semiconductor (MOS) with 256 words, 10 bits each. The ROM is programmed with the necessary beam blank/unblank dot patterns for video formation of all displayable characters within a 5-dot by 9-dot matrix on a terminal display screen.

INTERFACE CIRCUITS

Interface circuits, located on two cards in the logic module, provide for communications with a modem. This interface is asynchronous and is designed to operate with data bit serial signals compatible to EIA Standard RS-232-C such as with AT&T 103 series modems (or equivalent). The modem interface circuits are located on two printed circuit cards in the module (reference figure 1-4). The interface communicates at switch selectable rates of 75, 110, 150, 200, and 300 serial bits of data per second. The interface circuits perform all serial-to-parallel and parallel-to-serial conversion for 8-bit serial ASCII X3.4-1968 communication codes (the 8 bits include parity bit), modem control, and during transmission, executes the data clocking.

A printer channel accompanies the modem interface on the two interface cards. This channel accommodates a low-speed hardcopy printer (30 characters per second). Control circuits allow for printout of all characters in the display read/write memory (page print) or on-line printout of data as it arrives character-by-character in the read/write memory. The printer channel transmits 7-bit ASCII character codes to a printer bit serially. The channel circuits contain "printer-in-use" recognition circuits and differential amplifier driver/receivers which allow up to eight display terminals to share one printer.

EXPANDED MEMORY OPTION

An additional 640 characters of display read/write memory are available as an optional plug-in card (see Foreword). With this option in place, the logic module supplies character refresh for a 16-line display of 80 characters per line.

PHYSICAL, ELECTRICAL, AND ENVIRONMENTAL DATA

The following provides physical and electrical data for the display logic module.

Dimensions and Weight

Height: 10.8 in. (27.4 cm)
Width: 3.06 in. (7.77 cm)
Length: 10.0 in. (25.4 cm)
Weight: 4 lb (1.8 kg)

Environmental Specifications

Operating Temperature: +40°F to +120°F (+4°C to +49°C)
Operating Humidity: 10% to 90% - no condensation
Operating Altitude: -1000 ft to +10,000 ft (-305m to +3048m)
Storage Temperature: -30°F to +150°F (-34°C to +66°C)
Storage Humidity: 5% to 95% - no condensation
Storage Altitude: -1000 ft to +15,000 ft (-305m to +4572m)

Power Requirements

+5v (logic)
+12v (character memory)
-12v (logic)
0v (signal ground)

SECTION 2

OPERATION

This section describes controls and indicators, logic module interface, communication words, message formats, communication modes, programming procedures, and programming tips for the logic module.

CONTROL AND INDICATOR

Figure 2-1 shows the location of the control and indicator located on the logic module. Table 2-1 explains their functions.

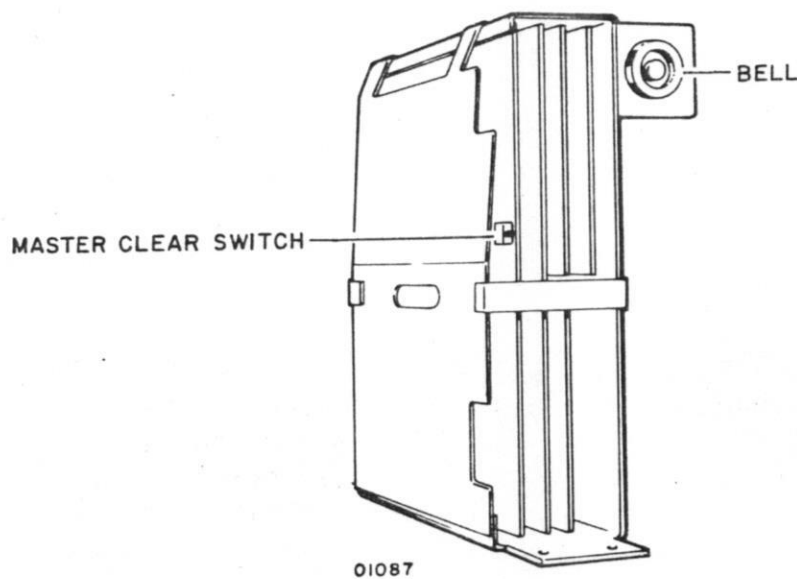


Figure 2-1. Location of Logic Module Control and Indicator

TABLE 2-1. LOGIC MODULE CONTROLS

CONTROL/INDICATOR	TYPE	FUNCTION
Master Clear	Momentary Pushbutton Switch	Returns all circuits to initial, unselected condition (for maintenance use only).
Bell	Audible-Tone Generator	Notifies operator that cursor is nearing the location in display refresh memory that corresponds to the end of a display line. Also alerts operator if logic module receives a Bell input control function.

MODULE INTERFACE

The following paragraphs describe modem and printer interface communications for the logic module.

MODEM INTERFACE

The basic module contains a quad-line-driver/receiver interface for communication between the module and an external modem. The interface operates at transmission rates of 75, 110, 150, 200, or 300 baud. The interface circuits provide for switch selection of one of these baud rates for transmission rate compatibility with external communications equipment.

This interface requires five control and data signal lines plus a signal ground line (see table 2-2). The interface signals conform to EIA Standard RS-232-C and CCITT recommendation V24. This means that, on the interface, a data signal line held more negative than -3 volts is a logical 1 (marking) and a control signal line held more negative than -3 volts is a logical 1 (off). Data lines held more positive than +3 volts are considered logical 0 (spacing) and control lines at over +3 volts are logical 0 (on).

These signals are for communication with AT&T 103 series (or equivalent) modem. The maximum cable length allowable for any of these signals is 50 feet. The following paragraphs define these signals and their operable voltage levels.

TABLE 2-2. INTERFACE SIGNAL LINES WITH EXTERNAL MODEM

J2 CONNECTION PIN	SIGNAL
34	Data Set Ready
35	Clear to Send
36	Receive Data
37	Request to Send
38	Send Data
32	Protective Ground
17	Signal Ground

Protective Ground

This line is connected to the frame of the terminal and is also connected to ground through the terminal's ac ground system. At the logic module, this line is connected to the chassis frame of the logic module.

Signal Ground

This signal is the voltage base from which the control and data signal voltage levels are referenced. This ground level is connected to the ac power ground in the display portion of the terminal.

Transmit Data

Data travels from the interface circuits to the modem via the Transmit Data line. When the interface is not transmitting data, the logic module holds the transmit data line to a logical 1 (more negative than -3 volts).

Receive Data

Data travels from the modem to the interface circuits via the Receive Data line. When the modem is not transferring data to the logic module, the modem holds the receive data line to a logical 1 (more negative than -3 volts).

Request to Send

The interface circuits hold the Request to Send line at a logical 0 (more positive than +3 volts) to initiate a transmit operation. The logical 1 state (more negative than -3 volts) on the Request to Send line signifies that the interface circuits are in a receive mode.

Clear to Send

The modem sets the Clear to Send line to a logical 0 (more positive than +3 volts) in response to the Request to Send signal from the terminal interface circuits. The Clear to Send line becomes a logical 0 within 8 to 210 milliseconds after the Request to Send signal is made positive (active) by the interface. Time variation occurs because of turnaround time of the common carrier. The Clear to Send line remains active until the interface drops the Request to Send line to negative (inactive). At this time, the modem drops the Clear to Send line (inactive) and the terminal interface circuits return to a receive communications mode.

PRINTER INTERFACE

The module is designed with a serial printer output channel accompanying the modem interface on the two interface cards. This channel accommodates a low-speed (up to 30 characters per minute) hardcopy printer. The printer control circuits included in the module permit either full-screen (page) printout or printout of data when displayed. The printer channel presents data to a printer on a 7-bit ASCII character word basis, bit-by-bit serially. All character codes 040₈ through 176₈ and the control codes for backspace (010₈), line feed (012₈), and carriage return (015₈) are intended for a printer. The printer channel circuits contain "printer-in-use" recognition and drive circuits which allow up to eight terminals containing display logic modules to share one low-speed printer.

Presence of a printer does not affect operation of the basic (8 line by 80 character) module or the expanded line option (16 line by 80 character) configuration except during a print operation, keyboard inputs to the module are disabled and the printer channel I/O signals are used by the module interface and control circuits to sequence data codes to the printer.

Table 2-3 identifies the required printer interface signals and figure 2-2 shows typical printer signal routing in a terminal. Figure 2-3 illustrates printer channel signal routing. The communication technique is bidirectional, differential, long-line driver/receiver combination thus each interface signal requires a negative (-) and a positive (+) line as a twisted pair. The total cable length that can be handled by these driver/receivers is 1500 feet. The following paragraphs describe printer interface line functions.

TABLE 2-3. PRINTER CHANNEL INTERFACE SIGNALS

INTERFACE CARD B1 CONNECTOR J2 PINS*	SIGNAL
8 and 27	Data Out +
7 and 26	Data Out -
3 and 22	Clock +
6 and 25	Clock -
14 and 15	Active +
11 and 30	Active -
4 and 23	Strobe +
5 and 24	Strobe -
10 and 29	Busy +
9 and 28	Busy -
16 and 17	Ground

* See figure 2-2 for illustration of parallel signal routing.

DISPLAY/KEYBOARD TERMINAL

DISPLAY LOGIC MODULE

INTERFACE
CARD B1

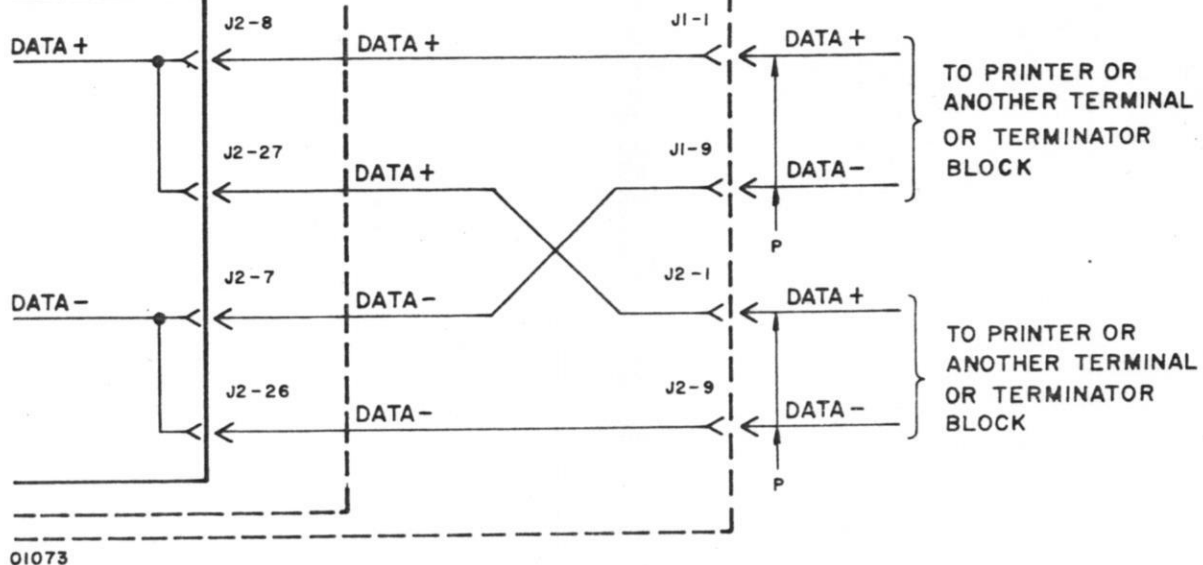
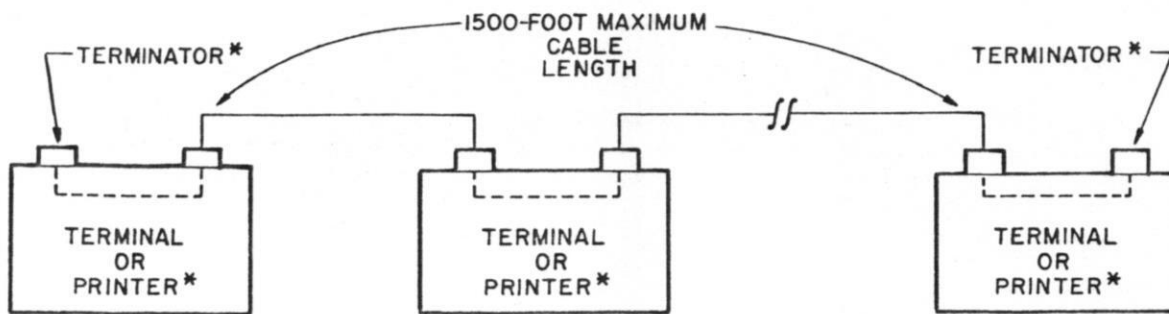


Figure 2-2. Typical Printer Channel I/O Signal Routing in a Terminal



* FROM ONE TO EIGHT TERMINALS MAY SHARE ONE PRINTER. PRINTER MAY BE LOCATED BETWEEN TERMINALS ON THE INTERFACE LINE OR ON EITHER END. TERMINATOR BLOCKS MUST BE INSTALLED ON THE SPARE CONNECTOR OF THE DEVICE (TERMINAL OR PRINTER) LOCATED ON EACH END OF THE INTERFACE.

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Figure 2-3. Terminal/Printer Interface

Data

Changing states of the positive (+) and negative (-) line pair signify binary bits of the ASCII X3.4-1968 compatible codes used for data transmission to the printer.

Data Bit "1" Condition	Pins 8 and 27 + current sinking
	Pins 7 and 26 - open
Data Bit "0" Condition	Pins 8 and 27 + open
	Pins 7 and 26 - current sinking

Clock

The logic module interface issues a clock signal via the clock line pair whenever it has a data bit condition established on the data line pair and sufficient time has elapsed for the signal to stabilize. The clock signal commands the printer to sample the data line pair for a valid data bit.

Clock (Logic "1" condition)	Pins 3 and 22 + current sinking
	Pins 6 and 25 - open
Not Clock (Logic "0" condition) . . .	Pins 3 and 22 + open
	Pins 6 and 25 - current sinking

Active

The active line pair indicates that one of the terminals connected to the printer is using the printer. Whenever a terminal is placed in use with the printer, the terminal's active line driver places the active line in a "being used" condition so that any other terminal connected to the printer recognizes that it is in use and not accessible by them.

Active (Logic "1" condition) Pins 14 and 15 + current sinking
Pins 11 and 30 - open
Not Active (Logic "0" condition) . . Pins 14 and 15 + open
Pins 11 and 30 - current sinking

Strobe

The logic module issues a strobe signal via the strobe line pair whenever it has completed sending all seven data bits of ASCII code to the printer via the data line and clock signal operations. The strobe signal commands the printer to translate and execute the complete data word it has just received.

Strobe (Logic "1" condition) Pins 4 and 23 + current sinking
Pins 5 and 24 - open
Not Strobe (Logic "0" condition) . . Pins 4 and 23 + open
Pins 5 and 24 - current sinking

Busy

The printer uses the busy line pair to indicate to all terminals connected to it that it is internally busy (during printhead return, etc.) and cannot receive data.

Busy (Logic "1" condition). Pins 9 and 28 - open
Pins 10 and 29 + current sinking
Not Busy (Logic "0" condition). . . Pins 9 and 28 - current sinking
Pins 10 and 29 + open

Ground

The ground signal line establishes a common reference ground for signal levels between terminals and the printer. Pins 16 and 17 carry the ground.

VIDEO INTERFACE

The video output from the display is via a co-ax cable. The signal is a composite video signal which provides beam blank/unblank information for the CRT. The signal line in the co-ax carries the composite video and the ground shield provides ground reference.

COMMUNICATIONS WORD

Module communications are with discrete words transferred bit serially. No block message formats are transferred.

WORD FORMAT

Communications with the module are bit serial, discrete word (no block message formats). Each word has 8 bits including one parity bit as shown in figure 2-4. A bit is transmitted and received as either a 1 or 0. Bit 2^0 is transmitted or received first. Bits 2^0 through 2^6 enable a total of 128 different codes of the ASCII X3.4-1968 code set (see tables 2-4 and 2-5).

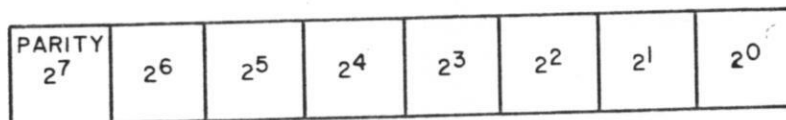


Figure 2-4. Word Format

A parity switch circuit allows selecting odd, even, or mark parity. The transmitting circuits count the number of 1's in bits 2^0 through 2^6 of a generated word. For odd parity setting; when the number of data bit 1's is even, a 1 is sent for bit 2^7 making the total number of 1's odd and if the number is odd, a 0 is sent for bit 2^7 leaving the total number of 1's odd. For even parity setting; when the number of 1's in bits 2^0 through 2^6 is even, a 0 is sent for bit 2^7 leaving the total number of 1's even and if the number is odd, a 1 is sent for bit 2^7 making the total number of 1's even. The receiving circuits use the parity bit to determine correct receipt of the word. Upon receipt, the receiving circuits count the number of 1's in all bit positions. When odd parity is set, the receiving circuits accept the word when the number of 1's is odd and generates a parity error character (177g ■) for display if the number of 1's is even. When even parity is set, the receiving circuits accept the word when the number of 1's is even and generate a parity error character for display if the number of 1's is odd. Since generating and checking the parity bit is not a programming function but is controlled by the transmitting and receiving circuits, octal codes shown in this section do not include the parity bit.

TABLE 2-4. DISPLAYABLE CHARACTER CODE REPERTOIRE (ASCII X3.4-1968)

OCTAL CODE	CHARACTER	OCTAL CODE	CHARACTER
040	Space	120	P
041	!	121	Q
042	"	122	R
043	#	123	S
044	\$	124	T
045	%	125	U
046	&	126	V
047	'	127	W
050	(	130	X
051	)	131	Y
052	*	132	Z
053	+	133	[Left Bracket
054	,	134	\ Reverse Slant
055	-	135	] Right Bracket
056	.	136	^ Circumflex
057	/	137	_ Underline
060	0	140	¯ Left Single Quote Mark
061	1	141	a
062	2	142	b
063	3	143	c
064	4	144	d
065	5	145	e
066	6	146	f
067	7	147	g
070	8	150	h
071	9	151	i
072	:	152	j
073	;	153	k
074	<	154	l
075	=	155	m
076	>	156	n
077	?	157	o
100	@	160	p
101	A	161	q
102	B	162	r
103	C	163	s
104	D	164	t
105	E	165	u
106	F	166	v
107	G	167	w
110	H	170	x
111	I	171	y
112	J	172	z
113	K	173	{ Left Brace
114	L	174	Vertical Line
115	M	175	} Right Brace
116	N	176	~ Equivalent or similar
117	O	177	■ Rub Out or Parity Error
		003	▲ (ETX) } Displayable
		016	< (S0) } Control
		017	> (SI) } Functions

TABLE 2-5. CONTROL FUNCTION CODE REPERTOIRE (ASCII X3.4-1968)

OCTAL CODE	DISPLAYABLE CHARACTER	NAME RESPONSE
000		NUL
001		
002		
003	▲	ETX - Displays Character at Cursor
004		
005		
006		
007		BELL - Activates Sonic Tone Alert (Bell)
010		BS - Cursor Backspace*
011		
012		LF - Line Feed (Cursor Down)*
013		
014		
015		CR - Cursor Return*
016	␣	SO - Begin Inverse Video and Display Character at Cursor*
017	␣	SI - End Inverse Video and Display Character at Cursor*
020		
021		
022		
023		
024		
025		Skip*
026		Reset*
027		
030		Clear*
031		Line Clear*
032		Cursor Up*
033		
034		FS
035		GS
036		RS
037		US

* Causes display operation when received by display logic module.

WORD CODES

Word codes transmitted and received by the logic module include ASCII X3.4-1968 displayable character codes and control function codes. Codes in the range 040g through 177g comprise the 96₁₀ character codes. Table 2-4 shows the character code repertoire. Codes 000g through 037g comprise the 32₁₀ control function codes. Table 2-5 shows these codes. Only twelve of the control function codes result in display logic module operations affecting the associated display/keyboard. These twelve codes are noted in table 2-5 and the purpose of each code is described in the following paragraphs. The remainder of the function codes shown in table 2-5 cause no internal logic module operation when received by the logic module circuits.

End of Text (ETX)

ETX code (003g) is entered in display memory and subsequently on the associated display screen to identify the end of a message.

Bell (BELL)

Bell code (007g) received by the logic module sounds the sonic alert located on the module.

Backspace (BS)

A backspace code (010g) moves the cursor (data entry point marker) one character position back without affecting displayable data codes stored in display refresh memory.

Line Feed (LF)

The line feed code (012g) generally advances the position of the cursor in display refresh memory to the same relative character position in the following display line. Displayable data stored in refresh memory is not affected unless the module is operating in scroll mode and the cursor is positioned for display in the bottom display line (8th line in basic machine and 16th line in expanded memory machine). When scroll mode is active and the cursor is in the bottom display line, a line feed function causes all displayable data to shift up one display line in refresh memory and the cursor returns to the first character position of the new bottom display line.

Cursor Return (CR)

The cursor return function (015g) moves the cursor to the first displayable character position of the display line it is in. Displayable data is not affected.

Begin Inverse Video (SO)

Begin inverse video code (016g) enters in display refresh memory and displays on the associated display screen at the present cursor position. Starting at this point, the display logic module outputs inverse blank/unblank composite video to the associated CRT display. This produces a display of black characters on a white background.

End Inverse Video (SI)

End inverse video code (017g) enters in display refresh memory and displays on the associated display screen at the present cursor position. Starting at this point, the display logic module ends inverse video output for the associated CRT display (if such existed due to a preceding start inverse video code).

Skip

The skip function code (025g) advances the cursor one character position in display memory. Displayed data is not affected unless the module is operating in scroll mode and the cursor is in the last character position of the bottom display line. In this case all data shifts up one display line and the cursor moves to the first character position of the new bottom line.

Reset

Reset code (026g) causes the cursor to return to the first character position of the top display line in refresh memory when scroll mode is not active. When scroll mode is active, reset code moves the cursor to the first character position of the bottom display line.

Clear

Clear code (030g) removes all information stored in refresh memory. The cursor then positions to the first character position of the top display line if scroll mode is not active. If scroll mode is active, the cursor positions to the first character position of the bottom display line.

Line Clear

The line clear mode (031g) causes removal in refresh memory of all data from the cursor position to the end of that line.

Cursor Up

The cursor up function code (032g) relocates the cursor to the preceding display line, same relative character position. Data in display refresh memory is not affected.

MESSAGE FORMATS

Messages are received and transmitted by the interface circuits of the logic module on asynchronous data-word-by-data-word basis. Table 2-6 shows the two message formats used. The message transfer rate is selected by the baud rate circuits. Rates of 75, 110, 150, 200, and 300 bits per second are available.

TABLE 2-6. MESSAGE FORMATS

RECEIVE DATA WORD FROM MODEM		TRANSMIT DATA WORD TO MODEM	
One Word	Stop (logical 1)*	One Word	Stop (logical 1)*
	Start (logical 0)		Stop
	Word Bit 0		Start (logical 0)
	1		Word Bit 0
	2		1
	3		2
	4		3
	5		4
	Word Bit 6		5
	Parity		Word Bit 6
	Stop (logical 1)*		Parity
	Start (logical 0)		Stop (logical 1)*
	Word Bit 0		Stop
	1		Start (logical 0)
	2		Word Bit 0
	.		1
	.		2
	Word Bit .		Word Bit .

* Receive data requires at least one stop bit between data words and transmitted data requires at least two stop bits between data words.

COMMUNICATIONS MODES

The display logic module receives or transmits data via the interface circuits.

RECEIVE COMMUNICATIONS

The logic module stores data in the refresh memory at any time it arrives via the communications modem. With an optional printer connected to the logic module's printer interface channel and the printer-on-line circuits active in the logic module, a hard copy is obtained of the data received for the refresh memory.

TRANSMIT COMMUNICATIONS

The logic module transmits data, ASCII character by character, as it is composed from an associated data entry keyboard. However, transmission and display of keyboard initiated data depends on the operating mode of the logic module interface circuits. Circuits operation is either remote or local mode, depending on the setting of the Local switch circuit.

Remote Operating Mode

Remote operating mode issued to transmit data between a terminal and remote equipment. The logic module is designed to transmit data in either of two different duplex modes depending on the setting of the Duplex switch circuit.

Full Duplex Operation

With full duplex setting, the display logic module interface circuits route all keyboard generated codes through the modem to a central processor and, under central processor program control, they must be returned to the logic module interface through the modem before any display occurs.

Although named full duplex operation, this method of communication is in effect an echo-plex operation since data entries echo through the central processor before appearing on the terminal's display screen. This mode of operation provides an excellent method for the terminal operator to check data transmission accuracy between the terminal and the central processor.

Half Duplex Operation

With half duplex setting, the logic module routes all displayable keyboard generated codes to an associated display screen in direct response to keyboard entry and the codes are also sent through the modem to remote telecommunications equipment.

Local Operating Mode

The logic module will not transmit keyboard data entries when operating in the local mode. This mode is primarily a test mode allowing an operator to check operation of the terminal containing the logic module and optional associated hardcopy printer without placing data transmissions on the telecommunications lines to remote communications equipment.

PROGRAMMING PROCEDURE

Since the display logic module operates with an asynchronous interface, programming data involves little difficulty. The following paragraphs outline programming the logic module with an external modem.

- 1) When the modem interface connection is established, the data set ready control signal line becomes active (more positive than +3 volts). See Modem Interface in this section.
- 2) Reference table 2-6 for the format of the receive data code. Speed of transmission of the serial data bits match that of the baud rate switch circuit in the logic module interface circuits.

PROGRAMMING TIPS

The following suggestions should be considered when programming for the display/keyboard.

- 1) Basic display memory configuration (no expanded memory option) accepts 640 displayable character codes (reference table 2-4). Further character entry rewrites on displayed data.
- 2) Expanded display memory configuration (expanded memory option included) accepts 1280 displayable codes (reference table 2-4). Further character entry rewrites on displayed data.
- 3) All displayable character codes are recognized by the logic module and displayed (reference table 2-4).
- 4) Only those control function codes recognized by the logic module, reference table 2-4, are intended for display action (or sonic tone in the case of the bell function). All others referenced in table 2-5 are ignored by the logic module when received.

- 5) Transmission rate (baud rate) of communications word code bits sent to the module must match the rate set by the baud rate circuit in the logic module (externally located manual switch).
- 6) Parity for communication words must match that set by the parity select circuit in the logic module (odd, even, or mark selected with an externally located switch).

SECTION 3

INSTALLATION AND CHECKOUT

This section describes crating, uncrating, installation and checkout procedures for the display logic module.

CRATING

Reusable shipping containers are used by the manufacturing facility for initial shipment. These containers and packing materials should be retained on site in the event it is necessary to return faulty modules to the repair facility.

Figure 3-1 illustrates packaging for the logic module.

UNCRATING

Refer to figure 3-1 and uncrate the logic module as follows:

- 1) Open the shipping container and carefully remove the logic module.
- 2) Carefully remove all exterior packing material.
- 3) Place the logic module on a counter or table intended as the work area.
- 4) Retain all packing materials and the reusable shipping container for future use.

PHYSICAL LIMITATIONS

Since the logic module is designed to fit and operate within specific display/keyboard terminal cabinets, mounting patterns and space required for mounting is not of concern for installation. Installation is merely a task of placing the module in the correct cabinet location (see Mounting Procedures, this section).

NOTES:

- 1) PLACE D-120 AIR CAP (FOLD ONCE)
IN BOTTOM OF CONTAINER
- 2) PACKAGE PER ILLUSTRATION AND
SEAL WITH 3/4" FILAMENT TAPE

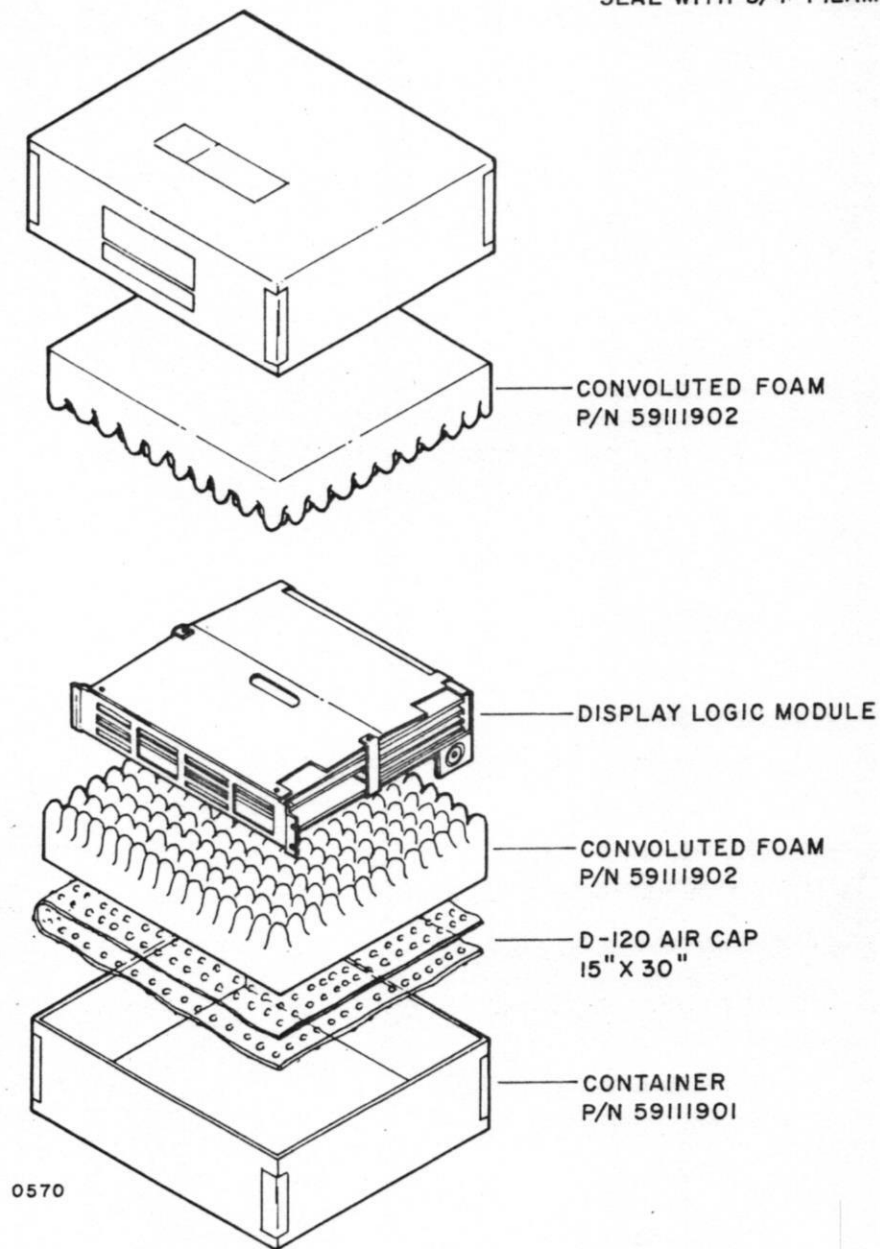


Figure 3-1. Display Logic Module Packaging

POWER REQUIREMENTS

The display/keyboard terminal using the logic module is designed to provide the cables and connectors to supply the power to the logic module cards. Connecting power to the logic module is easily accomplished by connecting existing cables at time of installation (see Mounting Procedures in this section).

The power connectors, located on each circuit card in the logic module, have a common configuration. Figure 3-2 shows this common pin configuration and the required voltages.

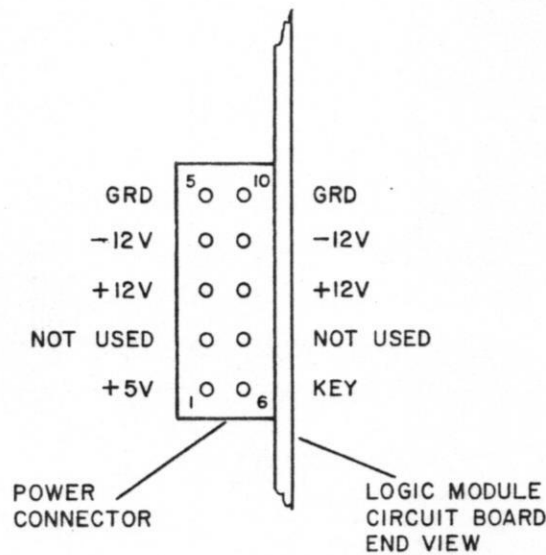


Figure 3-2. Power Connector Pins and Voltage Requirements

COOLING AND ENVIRONMENTAL REQUIREMENTS

Cooling requirements are determined by the display/keyboard using the logic module. Environmental requirements are described in Section 1.

MOUNTING PROCEDURES

To install the logic module, perform the following:

- Ensure that the ac power cable is not connected to the display/keyboard in which you are installing the logic module.
- Refer to the display/keyboard on-site customer engineering manual and install as specified. See figure 3-3 for illustration of installation.

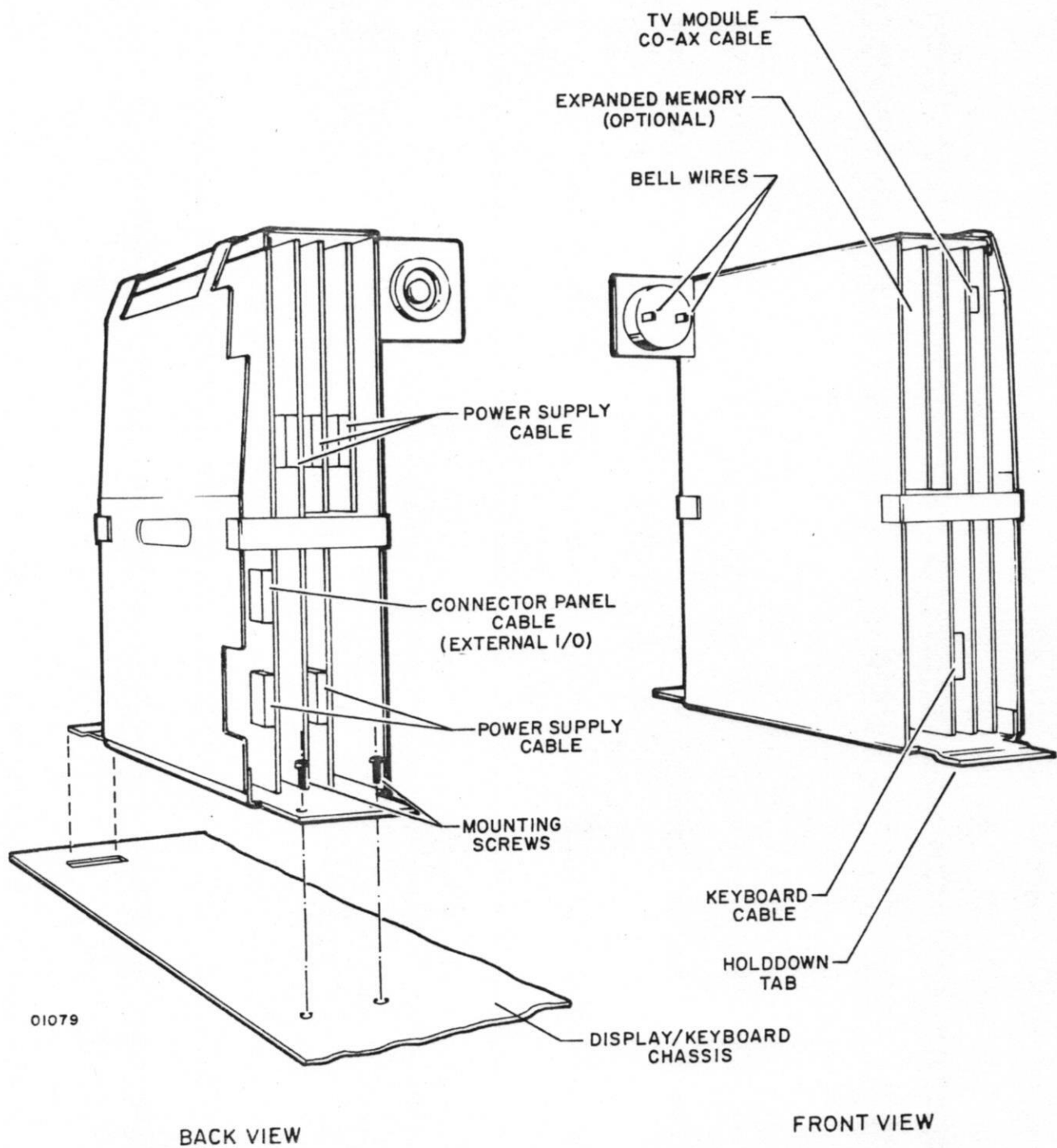


Figure 3-3. Typical Display Logic Module Installation

- Connect keyboard cable.
- Connect TV module co-ax cable.
- Connect connector panel (external I/O) cable.
- Connect power supply cables. Units designed to use the logic module contain six power connectors.
- Connect both bell wires.
- Ensure that the module is secured firmly by the holddown tab at the front and by two mounting screws at the back.

PREPARATION FOR USE

Before applying power to a logic module, check the following items.

- Inspect module cards and connectors for physical damage.
- Ensure that all card connectors are firmly seated.

CHECKOUT

Checkout is an operational performance check of a display/keyboard communications terminal containing the logic module. Since the logic module is designed to control all internal and interface operations of a display/keyboard, successful execution of all intended operations of the display/keyboard demonstrates proper operation of the logic module. Refer to the operators guide and reference manual for the specific display/keyboard operation descriptions.

If a fault occurs during checkout, use the information contained in the other sections of the manual to isolate and repair the circuit(s) responsible.

SECTION 4

THEORY OF OPERATION

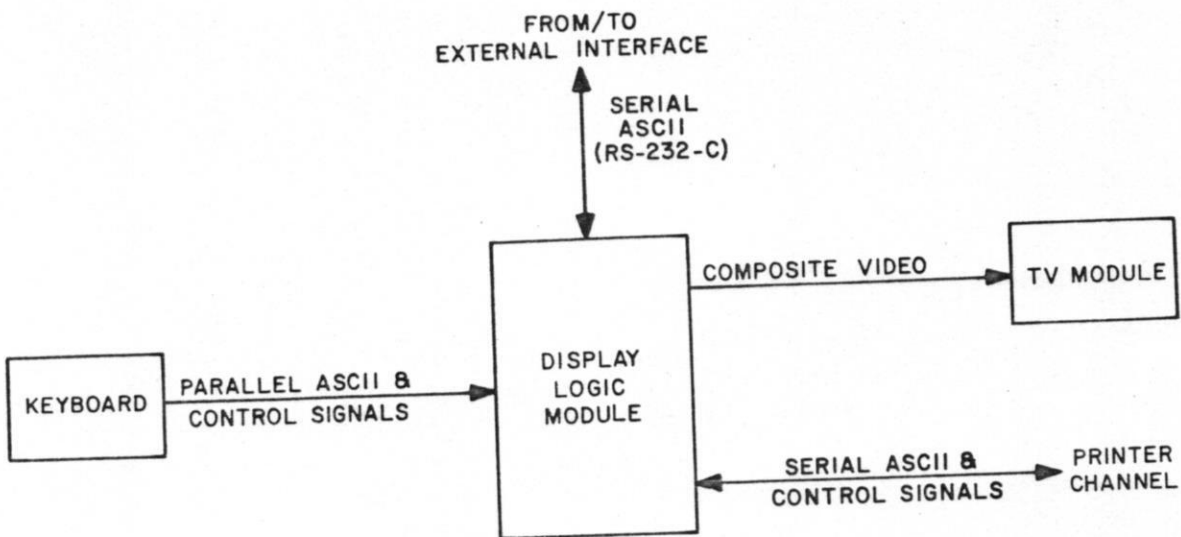
This section provides a comprehensive description of the functional operation of the display logic module. The first portion of this section, General, summarizes the overall operation and application of the module. The next portion, Logic Circuits, identifies and describes the purpose and operation of the functional circuits which comprise the logic module. This is done by text, block diagrams, timing charts, and references to the detail logic diagrams contained in Section 5, Diagrams. The remainder of this section describes sequences and functions performed within the logic module.

GENERAL

The logic module is designed to control all internal and interface operations of a conversational display/keyboard. As such, it performs the following general functions.

- Receives and executes display control functions (clear, move data entry point, etc.) from external interface.
- Receives displayable character codes from external interface and stores them for display refresh.
- Receives display control functions (clear, move data entry point, etc.) from an associated data entry keyboard and executes them and/or transmits them to external interface.
- Receives displayable character codes from data entry keyboard and stores them for refresh and/or transmits them to external interface.
- Supplies composite video signals to TV module for display refresh.
- Supplies ASCII codes to local printer interface to enable hardcopy printout of data.

Figure 4-1 shows the control application for which the logic module is designed.



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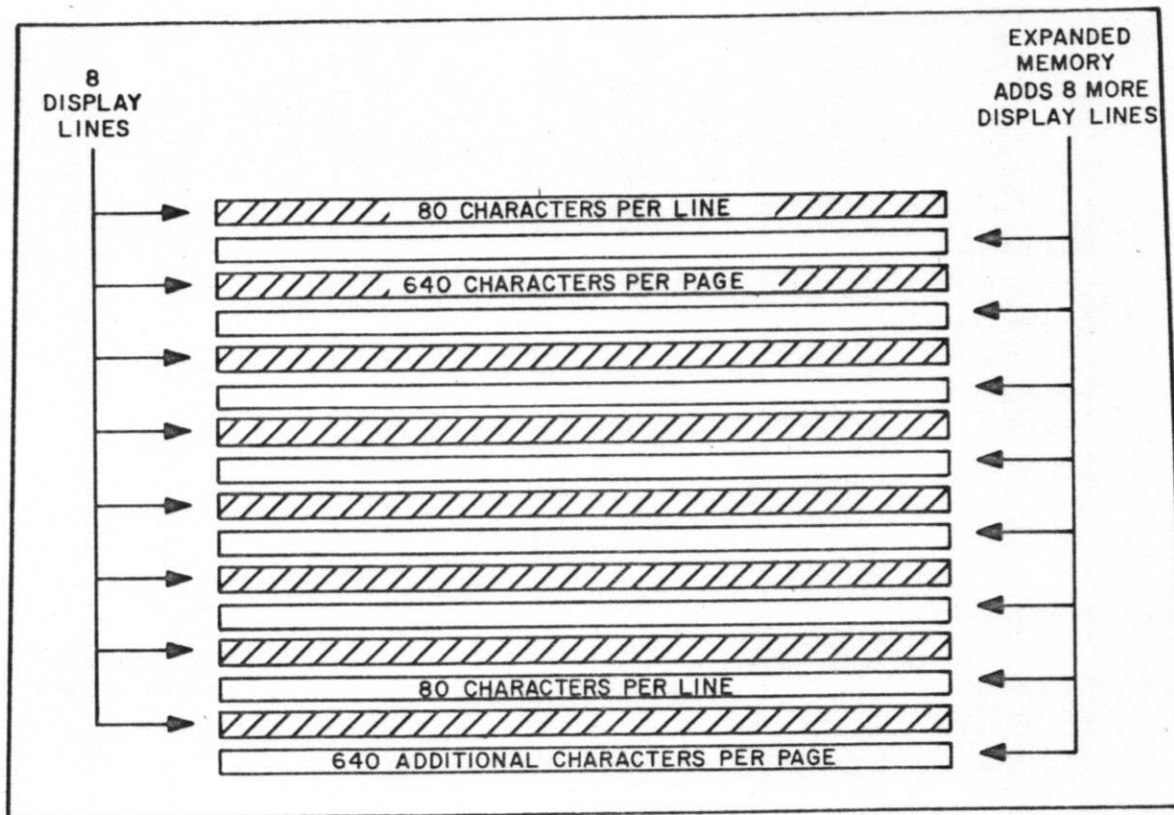
Figure 4-1. Display Logic Module Application

DISPLAY REQUIREMENTS

To aid in understanding the operation of the display logic module, the following paragraphs outline the characteristics of the CRT which depends on the logic module for composite video input.

DISPLAY LINE

Control for the CRT, to display 8 lines (16 lines optional with expanded memory) of characters, is supplied from the logic module. Each line has 80 character positions. All lines and all character positions may be used in a message to make a page with a maximum of 640 characters (or 1280 characters with expanded memory). Figure 4-2 shows the display lines on the display screen of a CRT associated with the logic module.



0109 4

Figure 4-2. Display Lines

SCAN LINE

Each display line of characters contains 12 horizontal scan lines. Figure 4-3 shows the relationship between characters and the scan lines which produce them. As the electron beam of the CRT makes one scan of the display screen, the logic module composite video output unblanks the beam to illuminate dots in only one row of each character matrix for each of the 80 character positions. As seen in figure 4-3, it requires seven scans to produce the dot patterns for the characters shown. The two scan lines immediately below the characters are used to produce dot patterns for other characters (lowercase "g," "p," etc.). The top and bottom scan lines provide a separation between characters in adjacent lines. Such line separation ensures visual clarity when characters display as black characters on a white background (inverse video: beam unblanks except on character dot patterns).

CURSOR

The logic module generates the composite video for display of the data entry cursor. The cursor underlines the character position on the screen where the next input or output action occurs. The cursor is a horizontal row of five closely spaced dots. The cursor displays in the next to the bottom scan line in a display line (see figure 4-3).

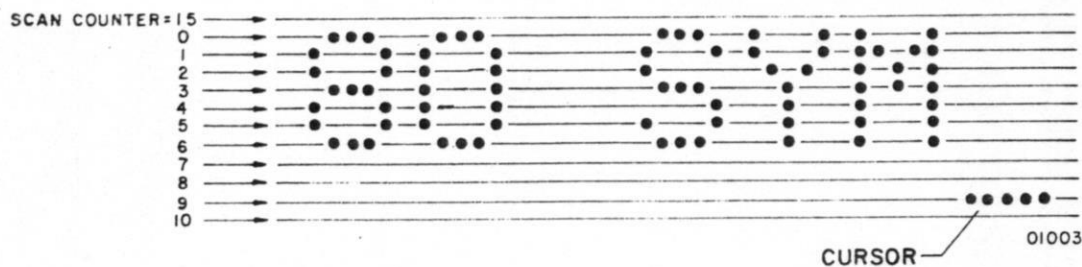


Figure 4-3. Character Dot Formations on Scan Lines

CHARACTER

The display uses a series of closely spaced dots to portray a character. The logic module supplies composite video signals such that the electron beam of the display CRT unblanks (turns on sufficiently to illuminate the phosphor coating on the face of the CRT) within a 5-dot by 9-dot matrix, as required to produce the dots required to form each character. All characters are 5 dots wide by 9 dots high. Figure 4-3 shows the dot patterns of several characters.

CONTROL LOGIC

The control logic circuits provide timing, counting, comparing, and routing of control signals within the logic module. These control signals determine the routing of display data between the modules shown in figure 4-1. A block diagram of the control and memory logic circuits are shown in figure 4-4. Figure 4-5 is a block diagram of the interface logic circuits. Reference these figures when reading the following circuit descriptions.

TIMING

A 20-MHz oscillator supplies the master clock timing for the display station. Its 50-nsec sine-wave output drives a flip-flop to produce a symmetrical square wave with a 100-nsec time period. This square wave, phase A, drives six more flip-flops to produce the timing chain of figure 4-5. The asymmetrical outputs of the timing chain have a 100-nsec pulse width and a 600-nsec time period. The 600-nsec time period is the time required to display one horizontal row of 5 dots (100 nsec/dot) in the character matrix plus a space between characters equal to 1 dot time (100 nsec).

CRT ELECTRON BEAM SYNCHRONIZATION

A television sync circuit uses the positional information (the counts) in the X counter, the Y counter, and the scan counter (enable vertical sync) to synchronize the CRT electron beam to the logic circuit timing.

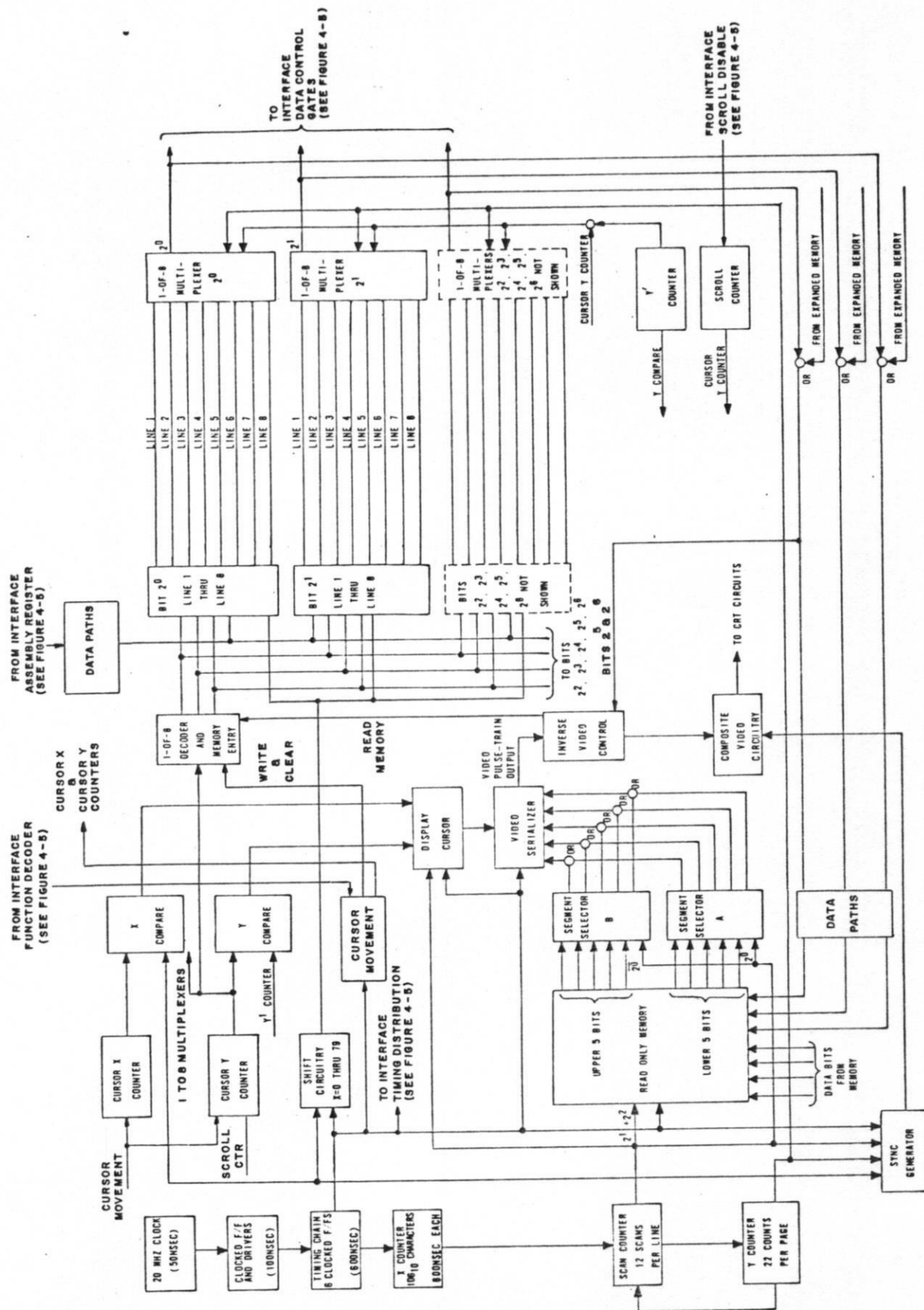
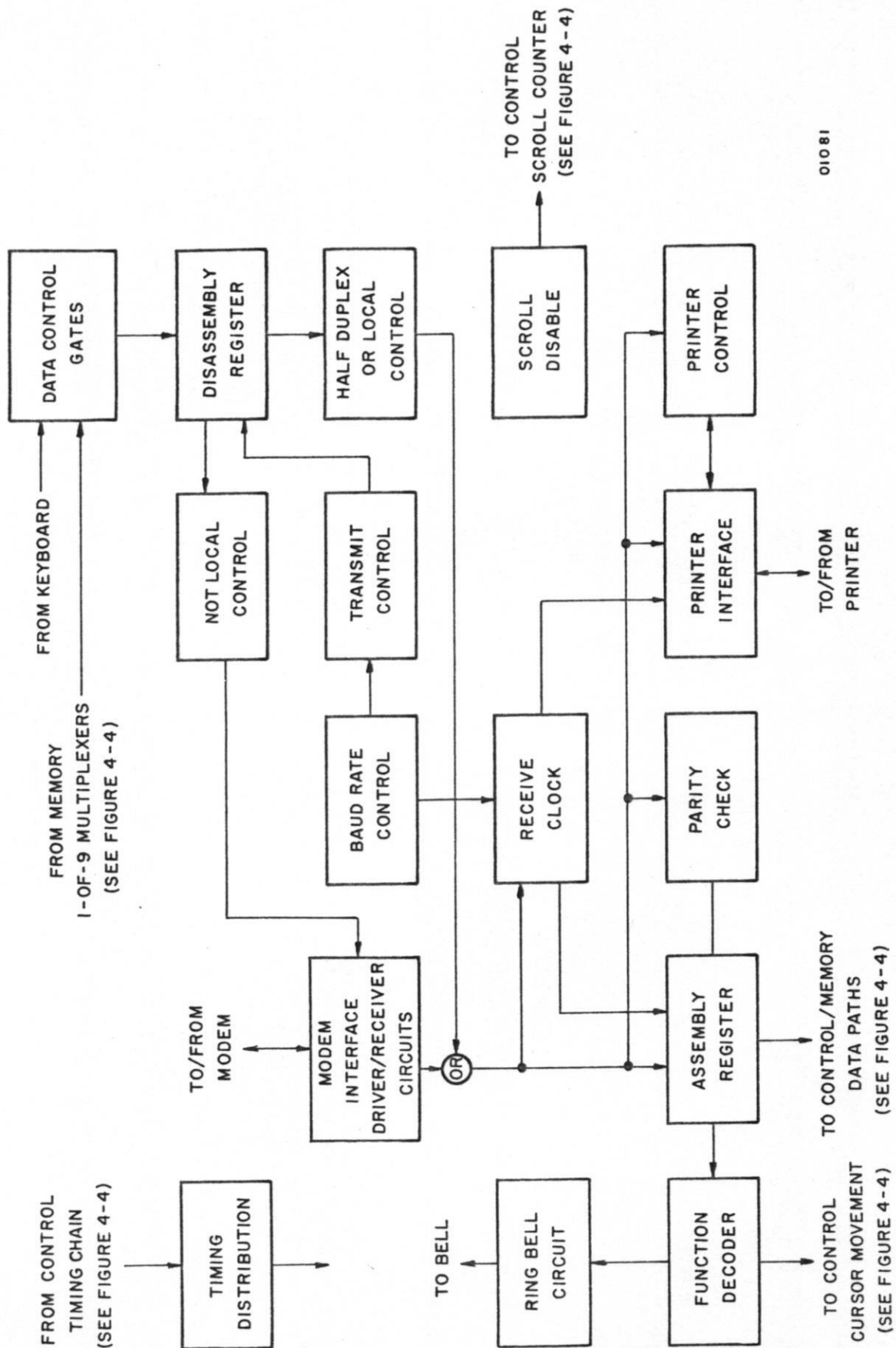


Figure 4-4. Control and Memory Logic Functions



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Figure 4-5. Interface Logic Functions

HORIZONTAL BEAM-POSITION INDICATOR

The horizontal beam-position indicator is the X counter. It advances every 600 nsec at the end of $\overline{T5}$. Figure 4-6 shows the relationship between the count in the X counter and the character positions in a display line. A count of zero indicates the first character position. A count of 79_{10} indicates the last character position. This gives 80 counts to equal the 80 character positions in each display line. If each character requires 600 nsec to display, then 80 characters require 48 μ sec (80×600 nsec). The time period of each scan line is equal to 106 character times or 63.6 μ sec (106×600 nsec). Because the 80 characters use 48 μ sec scan line time, the CRT electron beam has 26 character times to complete the horizontal retrace and return to the first character position of the display line. This time is 15.6 μ sec (63.6μ sec minus 48.0 μ sec). Table 4-1 lists the line timing scheme.

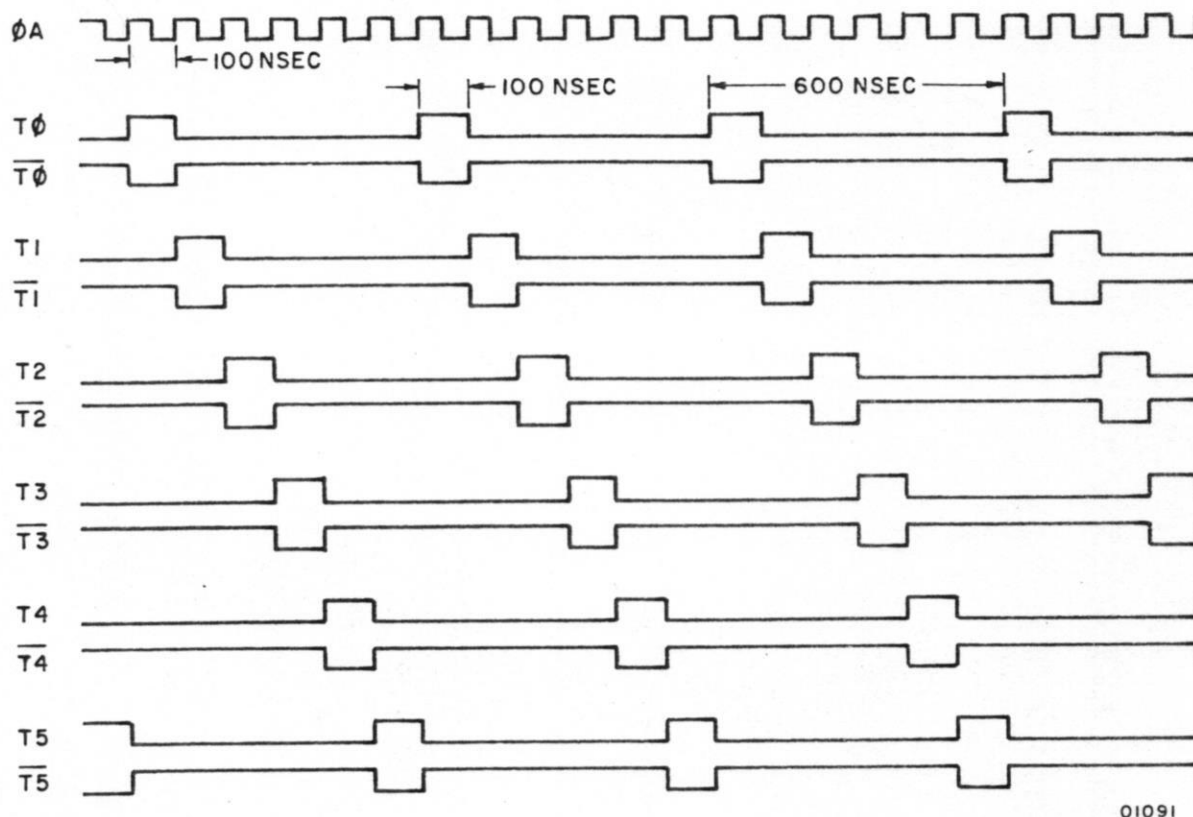


Figure 4-6. Timing Chain

TABLE 4-1. LINE TIMING SCHEME

TIME	LINE TIMING
100 nsec	1 dot time
600 nsec	1 character time (5 display dots plus a space of 1 dot)
63.6 μ sec	1 scan line (106 character times)
48.0 μ sec	Display time (in one scan line)
15.6 μ sec	Horizontal retrace time (26 character times)
2.2896 msec	Vertical retrace time (36 scan lines—includes beam settling)
16.6632 msec	1 frame (262 scan lines)

VERTICAL BEAM-POSITION INDICATOR

The vertical beam-position indicator is the Y counter. Figure 4-7 shows the relationship between the count in the Y counter and the display line positions.

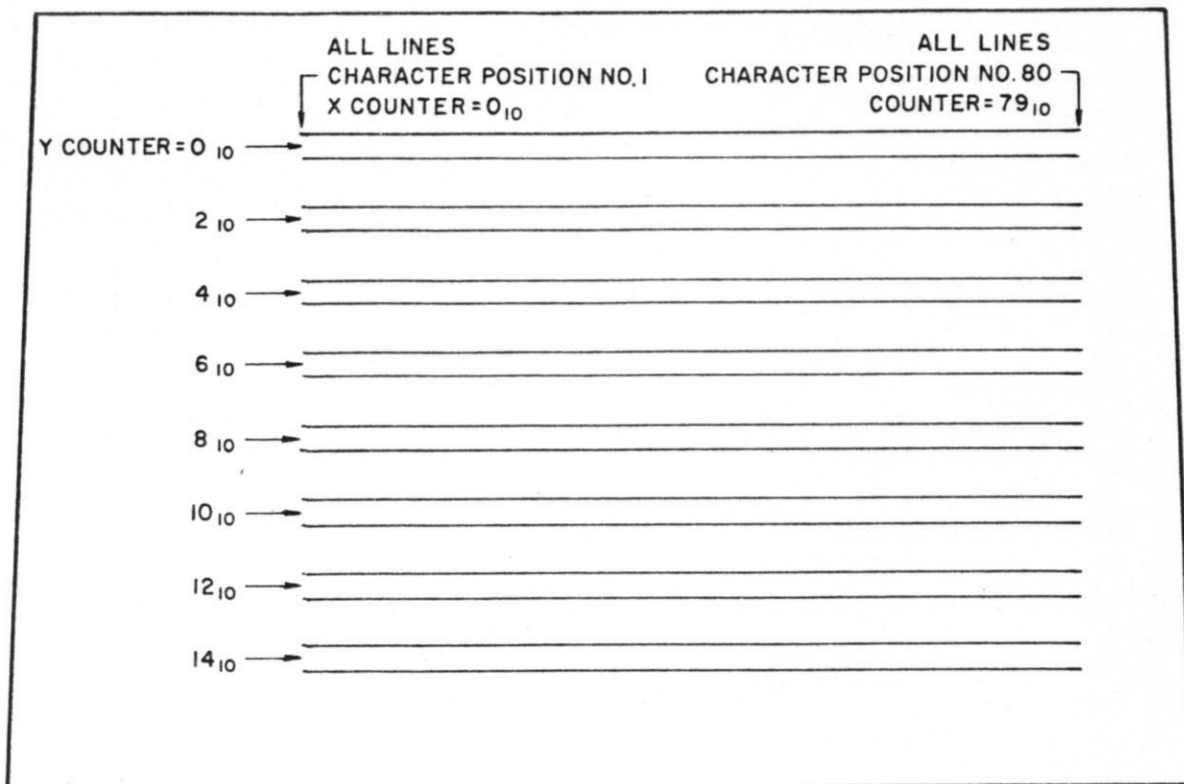
SCAN COUNTER

The scan counter keeps track of which scan line the electron beam is scanning in a display line. Figure 4-3 shows the relationship between the count in the scan counter and the scan lines. A new page or frame begins when: X counter = 10510, Y counter = 2110, scan counter = 810.

CURSOR POSITION INDICATOR

The cursor position indicator consists of the cursor X counter and the cursor Y counter. These counters contain the horizontal and the vertical axis coordinates, respectively, for the location of the cursor within the display. A compare (counts are equal) must exist between the X counter and the cursor X counter as well as between the Y counter and the cursor Y counter before the display station can display the cursor. This compare tells the station that the electron beam is at the cursor symbol position. Then, if the scan counter = 910, the beam unblanks to display the cursor.

The cursor position relates to the address in memory where the next entry or retrieval of a character code takes place. No compare occurs between the cursor Y counter and the Y counter for data entry or retrieval in memory. This is because a write or read operation makes the display line containing the cursor available at all times by enabling a 1-in-8 decoder for a write operation and by enabling a 1-in-8 multiplexer during a read. The cursor Y counter determines which of the read/write memory lines is selected. Then the station waits for an X compare before entering or retrieving a character code in the read/write memory.



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Figure 4-7. Character Position Display Coordinates

READ/WRITE MEMORY

The read/write memory furnishes the storage for the character codes which the logic module uses when refreshing the CRT display or when transmitting data to an external equipment. An 80-bit shift register stores one bit of each character's 7-bit code in an 80-character display line. Therefore, seven 80-bit shift registers store all the bits for one display line. The display contains eight display lines. This requires 56 shift registers (seven per line) to provide the necessary room for code storage. The basic building block in memory is a logic unit which contains four 80-bit shift registers. Because of this arrangement, the memory is referred to as a "Quad-80 Memory." Each shift register has its own internal recirculation circuitry. Recirculation (shifting) continues for as long as the shift register receives both a recirculation enable and a clock pulse from an external source. The X counter controls the clock pulse input. A clock pulse occurs every 600 nsec when the X counter contains a count of less than 80₁₀. This is the display time of each scan line. If shifting continues after the X counter reaches a count of 80₁₀, the data in memory would not display in its proper place in the next scan line of the display line. When performing a data entry in memory, the cursor X counter determines when the signal X compare enables the Write Line Select 1-of-8 decoder.

This decoder then uses the cursor Y counter input to its circuits to select one of the shift register groupings (display line). The next clock pulse leads the character code in memory.

When the read memory signal is active (the cursor X counter and X counter compare during a read operation), the display station transmits data to an external equipment beginning at the present cursor position. A read memory signal enables seven 8-input multiplexers. These multiplexers use the cursor Y counter inputs to their circuits to select one bit from one of the eight memory display line inputs to the multiplexer. This action places the 7-bit character code on the memory output lines.

READ-ONLY MEMORY

A preprogrammed read-only memory, ROM contains a character matrix which supplies the bits to build the video pulse train which unblanks the CRT electron beam to form a horizontal 5-dot row within the character matrix in the display line. The electron beam displays only one 5-dot row of each character in a display line for each horizontal scan line. The ROM has a separate matrix for each character in the repertoire of the logic module. As figure 4-8 shows, a code from the read/write memory determines the selection of the preprogrammed character matrix. When the synchronous timing signal read input (RI) arrives, the ROM logic samples the read/write memory code on the character matrix address lines to select the related character dot matrix in the ROM. Inputs scan 2^1 and scan 2^2 select one row in the character matrix to produce a 10-bit word output. Later, shortly after the synchronous timing signal read memory (RM) arrives, the ROM makes a 10-bit word available on its output lines. Because the electron beam displays only 5 dot positions of a character for each scan line, the 10-bit word furnishes the dot blank/unblank information for two adjacent scan lines of one character. Scan counter outputs scan 2^0 and scan 2^0 select one-half of the 10-bit word when the counter has an even count. The following odd count in the scan counter switches scan count bit 2^0 and enables the selection of the other half of the 10-bit word. The third advance of the scan counter enables the selection of a new row in the character matrix to form a new 10-bit word.

The ROM has two separate ROM assemblies. The primary ROM contains the preprogrammed character matrixes for the codes from 040_8 to 137_8 . The secondary ROM contains the matrixes for the character codes 003 , 016 , 017 , and 140_8 to 177_8 . The read/write memory applies its code to both the primary and secondary ROM's simultaneously. However, only one of the ROM's enables to sample the code. If the 2^5 bit and the 2^6 bit of the read/write memory code are logical 1's or are both logical 0's, the secondary ROM enables. If these bits are complementary, the primary ROM enables. The enabled ROM produces the 10-bit word output.

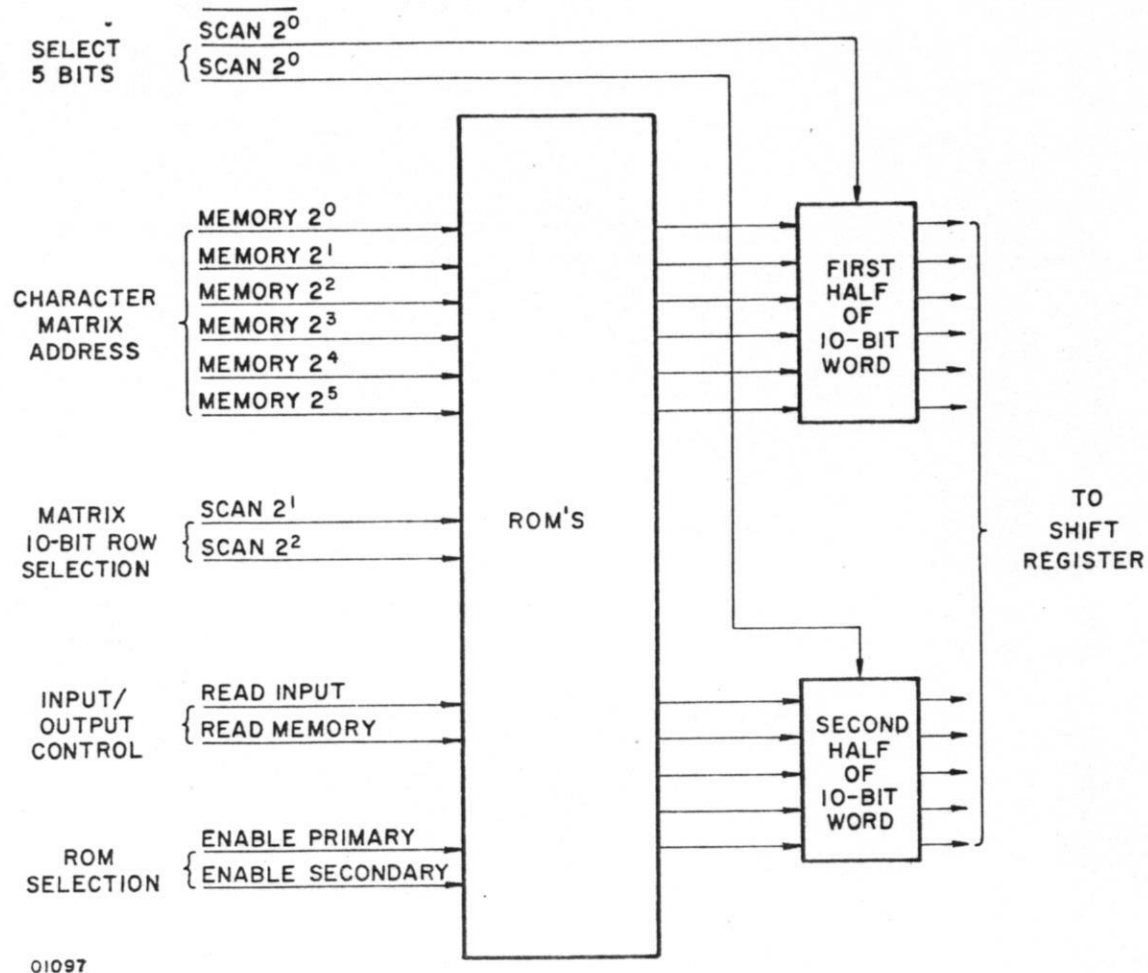


Figure 4-8. Read-Only Memory Signal Lines

VIDEO SERIALIZER

The 5-bit half of the 10-bit word output of the ROM parallel loads into a 5-stage video serializer shift register. The shift register receives six clock pulses to shift out the 5 bits in serial order to form the video pulse train. The pulse train which results produces one horizontal, 5-dot row, of a display line character matrix and a space between adjacent character matrixes. The space is equal to one dot time (100 nsec).

INVERSE VIDEO CONTROL CIRCUIT

The complementary outputs of the last stage of the video serializer each drive separate gates. Only one of these gates may pass the video pulse train at one time. Which one will pass the video pulse train depends on whether the data is within an inverted field (black on white). If the data is not within an inverted field, the set-side output of the last stage of the output shift register gates to give a display of white data on a black background. This is the normal display. If the data is within an inverted field, the clear-side output gates to give a display of black data on a white background.

This is an "inverted" display. The circuit which enables the gating of the inverted video signal is the inverse video control circuit.

COMPOSITE VIDEO DRIVER CIRCUIT

The composite video driver circuit combines the horizontal and vertical sync pulse output of the sync circuit with the video pulse train from the video serializer shift register. The output of this circuit drives the video amplifiers and deflection circuits of the CRT.

MEMORY CONTROL FF

The Memory Control ff permits the generation of the shift memory pulses, the setting of the White ff for a protected field display of black data on a white background, and the setting of the Display ff. The enable lasts from X counter = 0 through X counter = 79_{10} . This is the display time of a scan line.

DISPLAY FF

The Display ff allows refreshing of the screen display during display portion of the scan line. After display time, it makes certain the White ff is clear so the retrace is not visible.

X = 150_8 FF

The X = 150_8 ff sets to provide a logical 1 preset to all the stages of the X counter after the X counter reaches a count of 104_{10} . This permits the X counter to output the signal X terminal count (XTC) with the next advance of the counter. This signals the circuits that the CRT electron beam has completed the horizontal retrace and is ready to begin displaying the dot formations of the characters in the next scan line.

BLINK COUNTER

The blink counter clears the Display Cursor ff to prevent the display of the cursor so that the cursor blinks at a rate of approximately three times per second.

X COMPARE

The X compare circuit tells the other circuits that the count of the X counter equals the count of the cursor X counter. This means the CRT electron beam is at the horizontal axis coordinate of the cursor location. Together with the Y compare, it results in the display of the cursor. It is also used for the entry or retrieval of data in the read/write memory.

Y COMPARE

The Y compare circuit tells the other circuits that the count of the Y' counter equals the count of the cursor Y counter. This means the CRT electron beam is at the vertical axis coordinate of the cursor position. Together with the X compare, it results in the display of the cursor.

DISPLAY CURSOR FF

The Display Cursor ff sets to enable the forcing of all logical 0's in the video serializer shift register to produce the cursor pulse train.

PROTECTED FIELD FF

When a start inverse video code is detected in memory, the Protected Field ff sets to allow setting the White ff. This action gates the inverted video signal to give a display of black data on a white background.

HOLDOVER FF

The Holdover ff holds over the inverted field condition from one scan line to the next, until the end code clears out this inverted field condition. The Holdover ff then serves as the memory for an inverted field condition to allow the White ff and the Field ff to clear at the end of a display line and scan line, respectively, so the retrace is not visible.

WHITE FF

The White ff controls the gating of the complementary outputs of the last stage of the video serializer shift register. When clear, the White ff gives a normal display of white data on a black background. When an inverted field condition exists, it sets to produce a display of black data on a white background.

ROM ENABLE FF's

The ROM Enable ff's select either the primary or secondary ROM depending upon the logic state of the 2^5 bit and the 2^6 bit of the read/write memory character code. If bits 2^5 and 2^6 are logical 1's or both logical 0's, the ROM Enable ff's select the secondary ROM. If not, the circuit selects the primary ROM.

Y' COUNTER

During a refresh, the Y' counter selects the display lines in the read/write memory. Either a Y counter advance or a scroll operation allows the Y' counter to advance. A Y counter advance is the result of a normal refresh sequence. A scroll operation results in an extra advance of the Y' counter so that the displayed data shifts up one display line. This is because the Y' counter is now one display line ahead of the timing scheme and therefore enables the second line in the read/write memory while the CRT electron beam is scanning the top display line on the screen.

SCROLL FF

The Scroll ff acts if an input control function results in an attempt by the cursor to advance out of the bottom display line to a position in a nonexistent next lower display line. A scroll produces an extra advance of the Y' counter. Also, it sets the Clear Memory ff. All the data on the display screen shifts up one display line. The top line of data is lost and the bottom display line clears. The cursor resets to the first character position of the bottom display line. See paragraph headed "Y' Counter."

SCROLL COUNTER

The scroll counter advances with each scroll operation. The count in the scroll counter furnishes the reset count for the cursor Y counter. When a cursor resets to the first character position of the top display line, the count in the cursor Y counter is set equal to the count in the scroll counter. This makes the cursor appear in the top display line following the Y reset.

CURSOR Y CLOCK PULSE

The cursor Y clock pulse drives the cursor Y counter. During refresh, a clock pulse occurs only at T_5 to advance the Y' counter. However, during a cursor movement between display lines, a clock pulse occurs at T_5 and T_1 . This is because the basic memory and the expanded memory display lines interlace on the screen. This requires two clock pulses to move the cursor from one basic memory display line to the next basic memory display line.

INCREMENT CURSOR FF

If the circuit action requires the movement of the cursor, the Increment Cursor ff is the control point which the circuits use to control those operations that produce the desired movement of the cursor.

END OF OPERATION FF

When an input control function occurs, the End of Operation ff enables the clearing of the assembly register at T3 at the completion of the sequence.

WRITE SEARCH FF

When set, the Write Search ff allows an X compare to produce a write to the read/write memory. Also, it generates a busy signal.

READ SEARCH FF

When set, the Read Search ff allows an X compare to produce a read from the read/write memory. Also, it generates a busy signal.

CLEAR MEMORY FF

When set, the Clear Memory ff forces the space codes in the read/write memory. It may clear only one memory display line (input control functions line clear or new line, or any scroll) or it may clear the entire memory (master clear or input control function clear).

MASTER CLEAR OR CLEAR FF

Setting the Master Clear or Clear ff results in the filling of the read/write memory with space codes and the resetting of the cursor to the first character position of the top display line.

MASTER CLEAR

The master clear circuit allows two ways to master clear the circuits of the logic module. The first is an automatic master clear which occurs each time power is applied to the logic module. The second way is by pressing a Master Clear switch on the interface logic board.

WRITE LINE SELECT

During a write operation (Write Search ff is set), the Write Line Select 1-of-8 decoder selects a line in the read/write memory to permit a character code to be written into memory. When an X compare occurs, the decoder uses its inputs from the cursor Y counter to determine which memory line contains the cursor. This gates the character code to the input lines of the memory shift registers.

READ/WRITE MEMORY OUTPUT MULTIPLEXERS

During a read operation (Read Search ff is set), the read/write memory output multiplexers select a line in the memory to permit a character code to be read from the memory. When an X compare occurs, the multiplexers use the inputs from the cursor Y counter to select the memory line containing the cursor. This places the character code on the output lines of the memory. During a refresh, the multiplexers use the inputs from the Y' counter to select the memory lines in the order in which they are to be displayed.

END-OF-LINE TONE

During a data entry, when the cursor reaches character position 73 in a display line, a circuit enables an audible tone to signal this fact. Eight character positions remain from the present cursor position to the end of the line.

MODEM INTERFACE

The modem interface circuits consist of quad-line drivers and receivers which permit serial data flow between the logic module and an EIA Standard RS-232-C type communications modem.

When the modem interface receives a Data Set Ready signal, this means that the data set associated with the logic module is in a ready condition for communications.

To send data, the logic module generates the Request to Send control signal to initiate a transmit operation. In this condition, this signal line is more positive than +3 volts. In response to the Request to Send signal, the modem associated with the logic module makes the Clear to Send line more positive than +3 volts. The Clear to Send signal signifies that external communication connections are established. The logic module now may send serial data bits to the modem via the Send Data signal line.

When an associated modem has data for the logic module to receive, it sends it serially to the modem interface via the Receive Data signal line. Receive data takes precedence over other logic module operations. The logic module recognizes the presence of receive data when a start bit appears on the line.

BAUD RATE CONTROL

The logic module receives and transmits serial data at a bit-per-second rate (baud rate) according to the baud rate selection circuit. Rates of 75, 110, 150, 200, and 300 baud are available. The baud rate control determines the bit rate of the receive clock and the transmit clock.

LOCAL/REMOTE CONTROL

The logic module may be switched to local operation (send data disabled) by the local/remote control circuit. Local position prevents data entries from an associated keyboard from transmitting to an associated modem, but it does allow internal decoding for display operations. Remote selection allows send data.

DUPLEX CONTROL

The duplex control circuit determines whether data intended for transmission (send data) transmits only to the communications modem or if it transmits to the modem and also is decoded within the logic module for display operations. Full-duplex selection allows transmission to the modem only. Half-duplex selection permits transmission and decoding for internal operation. However, if the local/remote control circuit is selected for local operation all send data operations are disabled and all data entries initiated from a keyboard associated with the logic module are decoded for internal operations.

ASSEMBLY REGISTER

During a receive data function or send data function, when in local or half-duplex mode, the assembly register converts the serial data word to parallel. The assembly register is cleared when the data input is complete. Timing for data assembly is provided by the receive clock.

RECEIVE CLOCK

This clock begins running when the logic module receives a receive data start bit on its modem interface. The clock output synchronizes assembly register and printer interface operation.

PARITY CHECK CIRCUIT

Odd, even, or mark parity check selections are provided for receive data by the parity check circuit.

FUNCTION DECODER

The logic module uses one 1-of-16 decoder to decode control functions to be performed. The function decoder receives input from the assembly register. Functions recognized by the function decoder are shown in table 4-2.

TABLE 4-2. FUNCTION CODES

OCTAL CODE	FUNCTION
007	Bell
010	Backspace
012	Cursor Down
015	Return
025	Skip
026	Line Clear
030	Clear
031	Reset
032	Cursor Up

DISASSEMBLY REGISTER

The disassembly register converts parallel memory or keyboard data to serial data words suitable for transmission to a modem and/or to the printer channel.

TRANSMIT CLOCK

The transmit clock runs at the rate determined by the baud rate control. It synchronizes the transmit operation to the selected baud rate for data transfer at the modem interface or printer channel. It runs when keyboard data is not locked out and when a receive data operation is not in process.

PRINTER INTERFACE

Dual differential line receivers and dual differential line drivers comprise the printer interface. These circuits allow serial transfer of data to a printer associated with the logic module. When the line active signal is not active, the logic module is able to acquire the printer channel for its own use. This allows several devices to share a common printer. After the logic module has exclusive printer use, and if the printer is not sending a busy signal to the logic module, output to the printer is allowed. The logic module issues serial data to the printer via the data out signal line. When each bit of a data word is stable on the data out line, the logic module issues the clock signal to notify the printer. At the end of a data word, the strobe signal is sent to the printer. Each serial data word sent via the printer interface consists of one start bit, seven ASCII data bits and a parity bit.

PRINTER CONTROL

Printer control circuits enable the logic module to transmit data to an associated printer via the printer interface circuits. Block printout of entire display memory contents is available via a print key circuit. Continuous character-by-character printout of data received by the logic module from a communications modem or a keyboard is available by the printer's on-line circuit. Timing for printout is provided by the receive clock.

DISPLAY REFRESH

The refresh sequence prevents the decay of the displayed data. Also, it continually updates the display with the latest information present in the read/write memory. The refresh rate is sixty times per second with a 120-volt terminal and 50 times per second with a 220-volt terminal.

When the Read Memory signal is not active, the refresh is automatic. The refresh begins at the start of page which is: Y counter = 21_{10} , scan counter = 8_{10} , X counter = 105_{10} .

Just prior to the CRT electron beam beginning the sweep of the first scan line, at the upper left position of the upper left display character, the logic module circuits are set at: scan counter = 15_{10} , X counter = 0, and Y counter = 0.

To display a character, the logic module sends the timing signal RI (read input) to the ROM to allow the ROM to sample the character code at the output of the read/write memory. When the Read Memory signal is not active, the codes in the read/write memory appear at the inputs to the ROM automatically. If the read/write memory code has logical 0's or 1's in both bit positions 2^5 and 2^6 , the secondary ROM samples the code. If positions 2^5 and 2^6 are complementary, the primary ROM samples the code.

When the ROM samples the code from the read/write memory, the ROM also uses the scan counter inputs, scan 2^1 and scan 2^2 , to select a 10-bit row within the related character matrix in the ROM. Next, the ROM receives the timing signal RM (read memory). After a built-in delay, a 10-bit word appears at the output of the ROM. The shift registers of the read/write memory advance to output the code for the second character position in the top display line. The scan counter outputs, scan 2^0 and scan 2^1 , select one-half of the 10-bit word to form one horizontal row of five dots in the character formation on the display screen. When the scan counter advances, the second half of the 10-bit word is selected. The next advance of the scan counter selects one-half of a new 10-bit word.

The first half of the 10-bit word parallel loads into the video serializer output shift register. It is then shifted out in serial form to provide the video portion of the composite signal which is sent to the deflection circuits of the CRT. Six clock pulses shift out the 5 bits plus a space. This corresponds to six dot times. If this first code is an inverted field code, the Protected Field and the White ff's set to produce an inverted video signal (black data on a white background).

A video pulse train is thus formed for each horizontal row of dots for each character position in the scan line. When the X counter reaches a count of 79_{10} (80th character position), the display portion of the scan line ends. As the electron beam leaves the display portion of the scan line, the character code for the first character position in the display line shifts into the output position in the read/write memory. Further shifting of the read/write memory does not occur until the electron beam begins scanning the first position of the next scan line. Now, the X counter continues to advance.

When the X counter = 88_{10} , the sync circuit begins the horizontal sync pulse. Figure 4-9 shows the relationship between the duration of the sync pulse and the count in the X counter. The electron beam does not begin to retrace immediately, but it does so in time to return to the first character position of the next scan line as the X counter returns to a count of zero. At X counter = 98_{10} , the sync pulse ends. At X counter = 104_{10} , the X counter receives a logical 1 preset to all stages of the counter. At the next T5, the X counter parallel loads logical 1's in all its stages. This causes the X counter to output the XTC (X terminal count) signal.

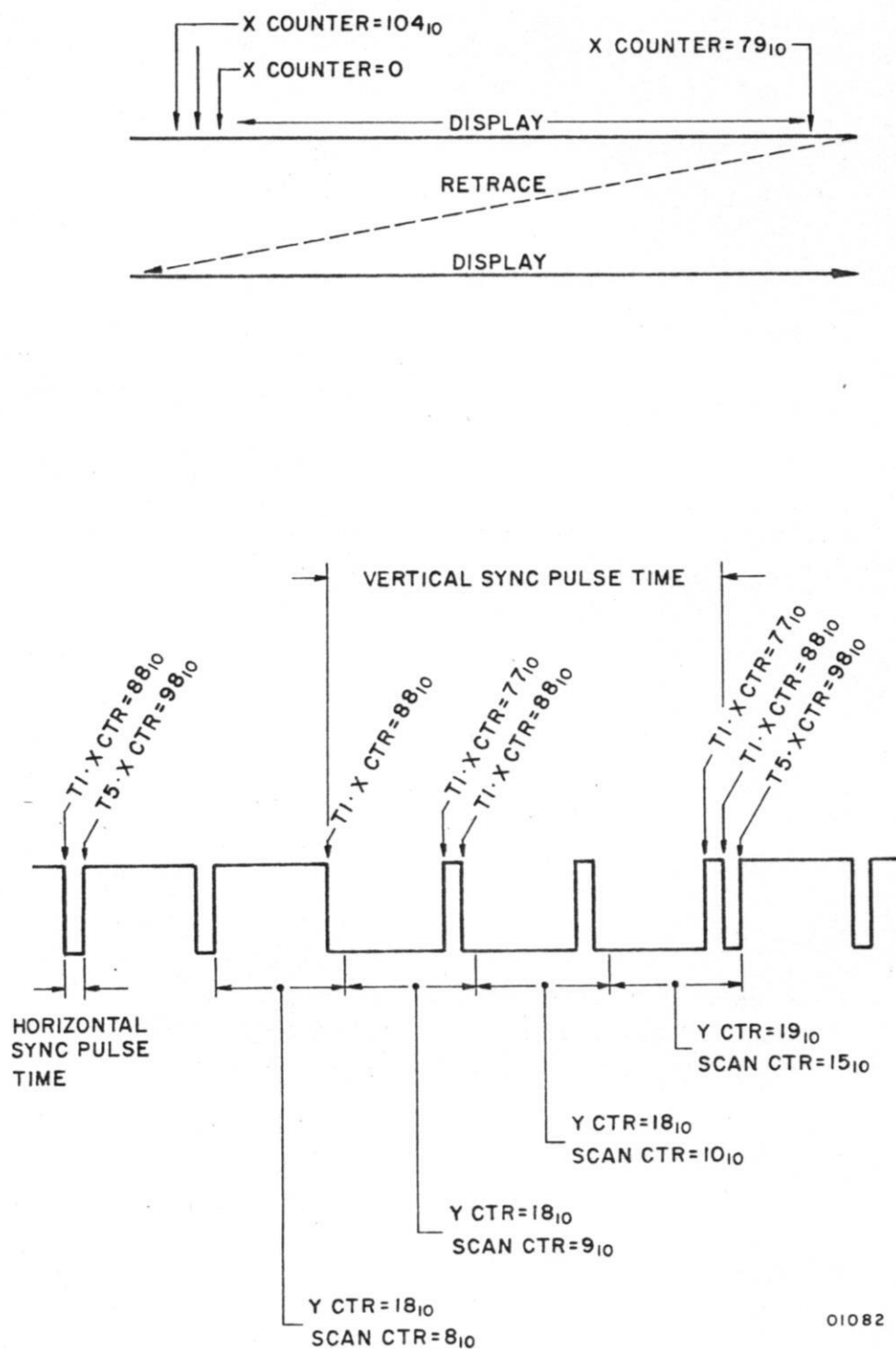


Figure 4-9. Horizontal and Vertical Sync Pulse Waveform

The scan counter then advances to the next line, and the X counter returns to a count of zero. The preceding action continues until the scan counter = 10_{10} . When this happens, the scan counter receives a logical 1 preset to all stages of the counter. At the next T_5 , the scan counter = 15_{10} as a result of the preset. The Y counter and the Y' counter advance so the next line in the read/write memory displays as the next lower line on the display screen. The preceding action repeats itself until the Y counter = 16_{10} . This means that the electron beam has advanced out of the last scan line of the bottom display line. The beam continues to scan down the lower part of the screen until the Y counter = 18_{10} and the scan counter = 9_{10} . This blocks the normal clearing of the sync circuit at the end of a horizontal pulse. This is done in preparation to starting the vertical sync pulse time. Figure 4-9 shows the relationship between the duration of the vertical sync pulse and the count in the X counter. Some time after the beginning of the vertical sync pulse, the electron beam starts to retrace vertically to a position above the first character position of the top display line. As shown in figure 4-9, four horizontal sync pulses occur during the vertical sync pulse time.

After the electron beam reaches the top, sufficient time is given to allow the beam to stabilize or to settle before the beam unblanks to begin displaying characters again. Approximately 35 scan times are used for this purpose.

DISPLAY CURSOR

The cursor results from the display cursor sequence. A blinking underline represents the cursor which indicates the next display location of a character on the display screen.

Before a cursor can display, four requirements must be met: 1) scan counter = 9_{10} , 2) Y counter < 16_{10} , 3) X compare, and 4) Y compare. This means that the CRT electron beam and logic circuit timing are at the position of the cursor. The cursor displays only in the eleventh scan line (scan counter = 9_{10}) of a display line (Y counter < 16_{10}) when the count in the X counter equals the count in the cursor X counter (X compare) and the count in the Y' counter equals the count in the cursor Y counter (Y compare).

When this occurs, the Display Cursor ff receives an enable to set. The next $\overline{T_3}$ sets the Display Cursor ff. This enables a gate which, in turn, supplies an input to permit setting a flip-flop that master resets all the stages of the video serializer output shift register. Next, T_1 passes through the gate to supply this enable. Then the phase A clock pulse sets the flip-flop that causes the master reset of all the stages of the video serializer. The next six phase A clock pulses shift the video pulse train out of the video serializer to produce the display of the cursor. When $\overline{T_5}$ occurs, the X counter advances by a count of 1 to end the X compare signal and, in so doing, ends the display cursor sequence.

INPUT/OUTPUT FUNCTIONS

The logic module interface circuits perform two functions 1) receive data and 2) send data. The data set ready signal must be active before the module will receive data. The Clear to Send signal must be active before the module will send data. In addition, the display station must not be busy receiving data or transferring data in the printer channel when a send data function is to be performed. If it is, the display station does not perform the function. The following pages describe what happens during these operations.

RECEIVE DATA

A receive data function commands the logic module to write any code on the logic module's receive data line into the read/write memory at the present cursor position, or to perform an internal control function such as clear, reset, advance cursor, etc.

Assuming that the Data Set Ready signal is active, the logic module is ready for a receive data sequence.

The receive data sequence begins when the receive data signal line becomes more positive than +3 volts indicating a start bit. The start bit is followed by 7 bits of data (least significant bit first) which are transferred serially into the assembly (shift) register. Following a receive data input, a receive sync pulse shifts the data in the assembly register allowing room for the next data bit. When the assembly register is filled, a flip-flop is set producing a data word assembled signal indicating the completion of the word assembly from serial to parallel. When bit 2^6 enters the assembly register, parity is checked. If both bits 2^5 and 2^6 are logical 0, the received data word is a function. If the word is not a function, it is stored in the refresh memory. A function word is decoded and acted upon.

Next the logic module generates an internal busy signal so the assembly register is not cleared until the present code sequence completes itself.

Storable Data

The circuits wait for an X compare to occur. When this happens, a decoder uses the information in the cursor Y counter to select the display line in memory which contains the cursor. With the logic circuit timing now at the position of the cursor, the next shift memory signal loads the received code into the read/write memory. The X compare ends and the cursor advances to the next character position.

Before completing the sequence, the logic module enters the character code above the new cursor position into the disassembly register. This requires another X compare. With this accomplished, the logic module ends the receive data sequence and the internal busy signal.

Function Data

A received function commands the logic module to move the cursor, erase data, start inverse video, or end inverse video.

Reset

The reset function commands the logic module to move the cursor to the first character position of the top display line without affecting the displayed data.

Assuming that the strobe out signal is active, that the station address is correct, and that the station is not busy, the display station enters the reset sequence. First, the cursor X counter is set equal to zero. The cursor Y counter is set equal to the scroll counter. The cursor is now at the first position of the top display line. Next, the display station generates a busy signal and clears the reset function code from the input buffer. Then, the code above the new cursor position is read from the read/write memory and is entered into the output buffer. Finally, the X compare and the busy signal end to complete the sequence.

Backspace

The backspace function commands the logic module to move the cursor one character position to the left in the display without affecting the displayed data. If the cursor is in the first position of any line and a backspace is performed, the cursor moves to the last position of the preceding line. If the cursor is in the first position of the top line and a backspace occurs, the cursor moves to the last position of the bottom display line.

To accomplish the backspace, the logic module forces the cursor X counter to count down by a count of one. If the cursor was previously in other than the first character position of any of the display lines 2 through 8, the cursor Y counter is not affected. The cursor now displays one character position to the left of its previous position. However, with a basic 8-line display memory, if the cursor was previously in the first character position of one of the display lines 2 through 8, the display station forces the cursor Y counter to count down by a count of 2. If the module contains the optional 16-line display memory, the cursor Y counter decrements by a count of 1. The cursor now displays in the last position of the previous display line. If the cursor was previously in the first character position of the first (top) display line, the

cursor Y counter counts down from a count of zero to a count of 15₁₀. The cursor now displays in the last position of the last (bottom) display line. Also, the logic module generates a busy signal, and clears the backspace function code from the assembly register. Then, when an X compare occurs, the station reads the symbol code above the new cursor position from the read/write memory in the output buffer. Finally, the X compare and the busy signal end to complete the sequence.

Line Clear

The line clear function commands the logic module to erase all the data from the present cursor position to the end of the line which contains the cursor without affecting the cursor.

A line clear operation clears the existing data from the present cursor position to the end of the display line by writing space codes into the read/write memory to replace those currently stored in memory. At the first X compare, the station begins a write to memory and, in so doing, generates an internal busy signal. The writing continues until a space code enters the last character position of the display line. Following this, the line clear function code clears from the assembly register. Next, the station reads the character code above the new cursor position from the read/write memory for storage in the disassembly register. Finally, the X compare and the busy signal end to complete the sequence.

ETX

The ETX function commands the logic module to store the ETX code in the read/write memory at the present cursor position. The ETX character (▲) displays at the cursor position. This code is used to identify the last data word in a message transmitted to an external equipment.

During an X compare, a write to the read/write memory enters the ETX code in the memory. This generates an internal busy signal. Then, the cursor X counter advances the cursor to the following position. During the next X compare, the display station reads the character code above the new cursor position from the read/write memory for storage in the disassembly register. Finally, the X compare and the internal busy signal end to complete the sequence.

Cursor Up

The cursor up function commands the logic module to move the cursor up one display line to a position directly above its present location. If the cursor is in the first display line when a cursor up sequence occurs, the cursor moves to the same relative position in the last line of the display.

If the module is not busy, it enters the cursor up sequence.

First, the cursor Y counter decrements by a count of 2 if the module contains the 8-line basic display memory and by a count of 1 if the module uses the 16-line expanded memory. If the cursor was in the top display line, it now displays in the same horizontal position in the bottom display line. If the cursor was not in the top display line, it now displays in the same horizontal position in the next upper (preceding) display line. The logic module now generates a busy signal and clears the cursor up code from the logic module assembly register. At the next X compare, a read from the read/write memory stores the character code above the new cursor position in the disassembly register. Finally, the X compare and the busy signal end to complete the sequence.

Clear

The clear function commands the logic module to erase all data from the display screen and to reset the cursor to the first character position of the top display line.

If the module is not busy, it enters the clear sequence.

During this sequence, a master clear returns all circuits to their initial condition. The most important of the results which follow the master clear are clearing the Y' counter, scroll counter, and cursor Y counter to zero; clearing the cursor X counter to zero at T5; and enabling all memory line inputs. The busy signal is active at this time. Next, the logic module writes space codes into all memory lines simultaneously. Then, the clear code clears from the assembly register. During the next X compare, a read from the read/write memory stores the character code above the new cursor position (the first character position of the top display line) in the disassembly register. Finally, the X compare and the busy signal end to complete the sequence.

Line Feed

The line feed function commands the logic module to move the cursor down one display line to a position directly below its present position without affecting the displayed data. If the cursor is in the bottom display line when a cursor down sequence occurs and scroll mode is active, all the data moves up (scrolls) one line. The top display line is lost, the bottom display line clears and the cursor resets to the first character position of the bottom line. If scroll is disabled, the cursor resets from the bottom line to the same relative position in the top line.

If the logic module is not busy, it enters the line feed sequence.

To move the cursor, the count in the cursor Y counter must change. If the cursor is not in the bottom display line, the cursor Y counter increments by a count of 2 if the logic module contains the basic 8-line display memory. If the module uses the 16-line expanded memory option, the counter increments by a count of 1. The cursor now displays in the same horizontal position of the next lower display line. The circuits generate a busy signal and then, clear the line feed code from the assembly register. During the next X compare, a read from the read/write memory stores the character code above the new cursor position in the disassembly register. Finally, the X compare and the busy signal end to complete the sequence.

However, if the cursor is in the bottom display line when the line feed function occurs, a scroll of the displayed data occurs. For a description of a scroll, see paragraph heading Scroll in this section.

Skip

The skip function commands the logic module to move the cursor one position to the right without affecting the displayed data. If the cursor is at the end of a display line when a skip sequence occurs, the cursor moves to the first character position of the next lower display line. If the cursor is in the last position of the bottom display line and scroll mode is active, when a skip sequence occurs, all the data moves up (scrolls) one line. The top line of data is lost, the bottom line clears, and the cursor moves to the first character position of the bottom display line. If scroll is disabled, the cursor resets to the first character position in the top display line.

If the module is not busy, it enters the skip sequence.

To accomplish a skip, the cursor X counter advances by a count of one. If the cursor was not at the end of a display line, it now displays one character position to the right of its previous position. The station generates a busy signal and clears the skip code from the assembly register. At the next X compare, a read from the read/write memory stores the character code above the new cursor position in the disassembly register. Finally, the X compare and the busy signal end to complete the sequence.

However, if the cursor is the last character position of the bottom display line when a skip occurs, a scroll of the displayed data occurs. For a description of a scroll, see paragraph heading Scroll in this section.

SEND DATA

A send data sequence occurs when a keyboard strobe is received by the logic module, the module is not in a receive data sequence, the Clear to Send signal is active, and the disassembly register is not active (key released and code from keyboard in disassembly register). The code is serially placed on the Send Data line from the disassembly register under control of the transmit clock. The start bit is sent first.

to tell the external equipment that a code is forthcoming. The code is sequenced on the Send Data line with the least significant bit first. The code goes out to remote equipment when the logic module is operating in either full- or half-duplex modes, providing it is not in local mode. Codes in this fashion do not enter display memory nor can they cause function operations within the module.

In local or half-duplex mode, keyboard input codes loop back from the disassembly register to the assembly register. At the assembly register, bits 2⁵ and 2⁶ are checked. If they are both logical 0, the code is a function. If either bit is a logical 1, the code is a displayable character. At this point, the keyboard data is treated the same as receive data received from the remote interface.

Whenever keyboard input codes loop back to the disassembly register, they are translated for being a displayable code or performable function code. They are treated in the same manner as if received from remote interface via the Receive Data line as described in Receive Data in a previous portion of this section.

Only one code is sent (or looped when local) per keyboard strobe.

SCROLL

A scroll is a switch selectable automatic sequence. It occurs if the cursor is in the bottom display line when the logic module receives the line feed code or any code which moves the cursor beyond the last character position in the bottom display line (e.g., last character and skip or last character and any displayable character received).

All the displayed data moves up one display line. The top line of data moves off the screen and is lost. The bottom display line clears, and the cursor moves to the first character position of the bottom display line.

At the beginning of a scroll sequence, the Y' counter and the scroll counter advance by a count of two if the logic module contains the basic 8-line display memory. It advances by a count of one if the module contains the 16-line expanded memory. This places the Y' counter ahead in the timing scheme so it is displaying the second line in the read/write memory as the first line of data on the display screen. The station uses the scroll counter to keep track of this special advance so the cursor can be reset to the first display line, when required. In those sequences requiring the cursor be reset to the first display line of the display, the cursor Y counter is set equal to the count in the scroll counter.

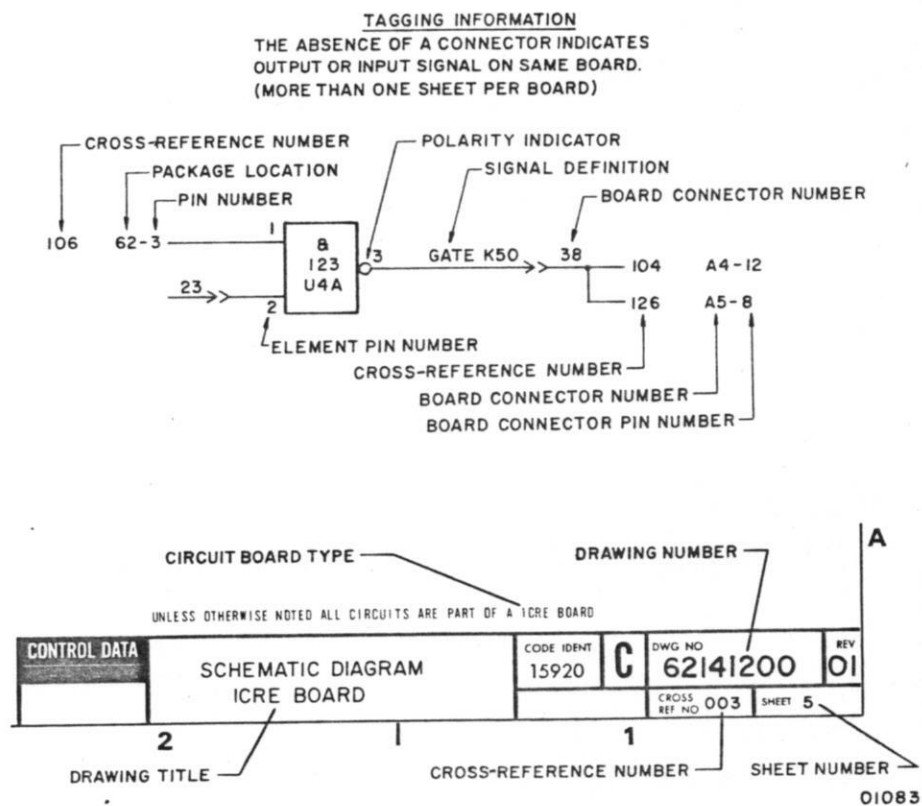
Following the advance of the Y' counter and scroll counter, the cursor X counter clears to zero. The cursor now displays in the first character position of the bottom display line. Beginning with the X counter = 0, the station writes space codes into the line in the read/write memory that corresponds to the bottom display line on the screen. After the X counter advances beyond the 80 character positions of the display line and reaches a count of 104_{10} , the logic module goes on to clear the received code from the assembly register. Then, at the next X compare, a read from the read/write memory displays the character code above the new cursor position. Finally, the X compare and the busy signal end to complete the sequence.

SECTION 5

DIAGRAMS

To help understand operation, maintenance, and troubleshooting of the logic module, this section supplies a key to symbols, logic circuit diagrams, and a printed circuit board interconnection diagram. A backup page gives a detailed explanation for each logic circuit diagram.

Figure 5-1 shows the identifying information contained on the logic diagrams.



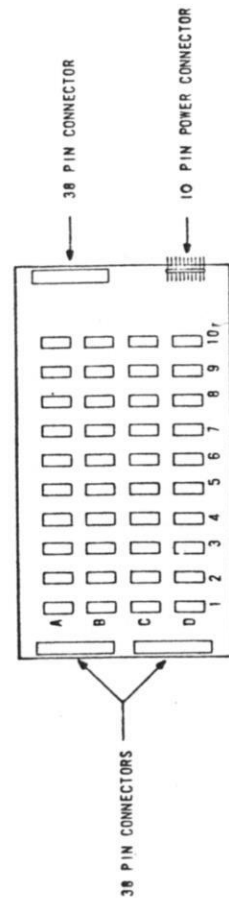
SHEET REVISION STATUS				REVISION RECORD			
REV	CD	DESCRIPTION	DATE	CHKD	APP		
01	00000-20	CLASS 5 RELEASE					
02	553	REVISED PER ECO					
03	652-4	RELEASED CLASS 5					

SHEET NO	CROSS REFERENCE NUMBER	REV	LOGIC DIAGRAM TITLE
1		A	LOGIC DIAGRAM CONTROL SHEET
2		A	KEY TO SYMBOLS
3		A	KEY TO SYMBOLS
4		A	KEY TO SYMBOLS (129, 140, 141)
5		A	KEY TO SYMBOLS (142, 143)
6		A	KEY TO SYMBOLS (144, 145)
7		A	KEY TO SYMBOLS (146, 147)
8		A	KEY TO SYMBOLS (158)
9		A	KEY TO SYMBOLS (159)
10		A	KEY TO SYMBOLS (162)
11		A	KEY TO SYMBOLS (166)
12		A	KEY TO SYMBOLS (167)
13		A	KEY TO SYMBOLS (176)
14		A	KEY TO SYMBOLS (183)
15		A	KEY TO SYMBOLS (187, 191)
16		A	KEY TO SYMBOLS (188, 189)
17		A	KEY TO SYMBOLS (193)
18		A	KEY TO SYMBOLS (201)
19		A	KEY TO SYMBOLS (240)
20		A	KEY TO SYMBOLS (500)
21		A	KEY TO SYMBOLS (501)
22		A	KEY TO SYMBOLS (700)
23		A	KEY TO SYMBOLS (900, 901)
24		A	BASIC CONFIGURATION, PRINTED CIRCUIT BOARD INTERCONNECTION DIAGRAM
25		A	BASIC MEMORY DATA PATHS
26		A	MEMORY TIMING, DISPLAY TIMING, * CONTROL
27		A	BASIC CONTROL RING COUNTER
28		A	BASIC CONTROL SCAN AND Y COUNTERS
29		A	BASIC CONTROL CURSOR X COUNTER
30		A	BASIC CONTROL CURSOR Y COUNTER
31		A	READ ONLY MEMORY AND VIDEO SERIALIZER
32		A	BASIC CONTROL PROTECTED FIELD
33		A	BASIC CONTROL SCROLL AND Y* COUNTER
34		A	BASIC CONTROL CURSOR MOVEMENT
35		A	BASIC CONTROL DATA PATHS, BASIC CONTROL CURSOR MOVEMENT
36		A	BASIC CONTROL X COUNTER
37		A	SIGNAL IDENTIFIER IFDE BOARD
38		A	DATA SET DRIVERS AND RECEIVERS
39		A	PRINTER BLOCK TRANSFER CONTROL

SHEET NO	CROSS REFERENCE NUMBER	REV	LOGIC DIAGRAM TITLE
40	102	A	DISASSEMBLY REGISTER
41	103	A	CURSOR CONTROL
42	104	A	PRINTER CONTROL AND DATA CONTROL
43		A	SIGNAL IDENTIFIER SHEET 2ASD BOARD
44	200	A	BASIC MEMORY CONTROL 8 LINES
45	201	A	MEMORY INPUT
46	202	A	MEMORY MUX 2 ⁵ & 2 ⁶
47	203	A	MEMORY MUX 2 ³ & 2 ⁴
48	204	A	MEMORY MUX 2 ¹ & 2 ²
49	205	A	MEMORY MUX 2 ⁰
50	206	A	MEMORY OUTPUT
51		A	SIGNAL IDENTIFIER SHEET 0JMD BOARD
52	300	A	TRANSMIT CLOCK
53	301	A	RECEIVE CLOCK
54	302	A	INPUT TIMING AND FUNCTION DECODES
55	303	A	ASSEMBLY REGISTER
56		A	SIGNAL IDENTIFIER SHEET 1CDE BOARD

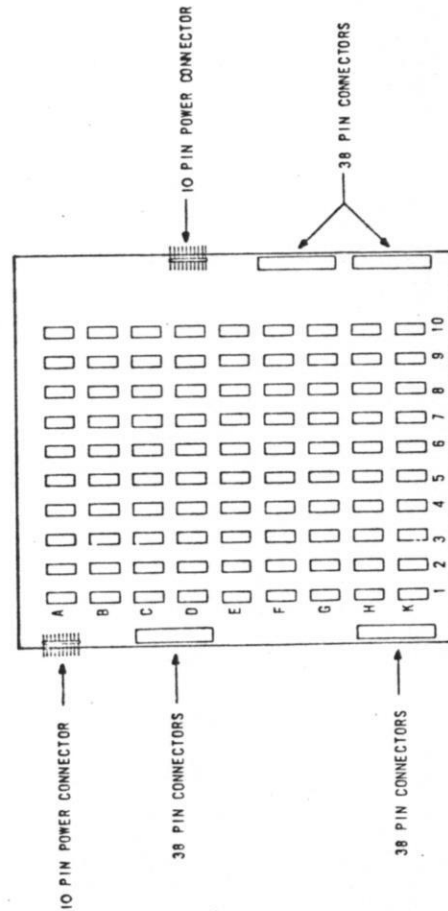
REFERENCE DRAWING		CONTROL DATA		TITLE	
		CC5A4-A		LOGIC DIAGRAM CONTROL SHEET	
FIRST USED ON		DWN		2-22-72	
		CHKD		2-22-72	
		ENGR		2-22-72	
		MFG		2-22-72	
		APPR		2-22-72	
COMPONENTS EXCEPT AS NOTED				CODE IDENT	
TOLERANCE		VALUE		15920	
RIS				DRAWING NO	
CAP				C 62164300	
				SCALE	
				SHEET 1 OF 56	

THE FOLLOWING DIAGRAMS SHOW ALL THE CIRCUITRY ON EACH PRINTED CIRCUIT CARD AND THEIR INTER CONNECTIONS. BECAUSE OF THEIR SIZE MORE THAN ONE LOGIC DIAGRAM MAY BE REQUIRED FOR EACH BOARD. EACH SYMBOL ON THE DIAGRAM REPRESENTS AN INTEGRATED OR DISCREET COMPONENT ON THE BOARD. EACH SYMBOL REFLECTS THE COMPONENT TYPE THE LOGIC FUNCTION PERFORMED AND THE COMPONENT LOCATION ARE WITHIN A ALPHANUMERIC MATRIX ON THE BOARD.



PACKAGE LOCATION ON BOARD

THERE ARE 40 LOCATIONS ON THIS BOARD. ONE AXIS IS LABELED A, B, C, AND D, AND THE OTHER AXIS IS LABELED 1, 2, 3, 4, 5, 6, 7, 8, 9, AND 10.



PACKAGE LOCATION ON BOARD

THERE ARE 90 LOCATIONS ON THIS BOARD. ONE AXIS IS LABELED A, B, C, D, E, F, G, H, AND K, AND THE OTHER AXIS IS LABELED 1, 2, 3, 4, 5, 6, 7, 8, 9, AND 10.

FIGURE 1

KEY TO SYMBOLS

CODE IDENT	DWG NO	REV
15920	C 62164300	A
	CAD33	SHEET 2

GENERAL LOGIC SYMBOL INFORMATION

INTEGRATED CIRCUIT LOGIC SYMBOL

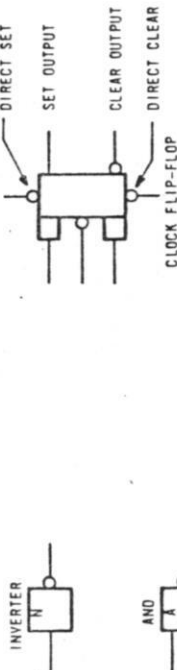
LOGIC FUNCTION IDENTIFIER
ELEMENT TYPE
PACKAGE LOCATION ON BOARD

ELEMENT TYPE

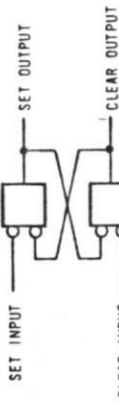
ELEMENT TYPE INFORMATION
IS ON THE FOLLOWING KEY
TO SYMBOLS SHEETS

LOGIC FUNCTION IDENTIFIER

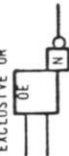
A = AND
OR = OR
JK = JK FLIP-FLOP
OE = EXCLUSIVE OR
N = INVERTER
E = EXTENDER
T = LINE TRANSMITTER
R = LINE RECEIVER



EXTERNALLY WIRED FLIP-FLOP

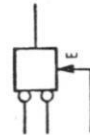


EXCLUSIVE OR

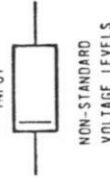


EXTENDER INPUT

AN EXPANDER ELEMENT
OR A DIODE MAY BE
USED ON AN EXTENDER INPUT



INPUT

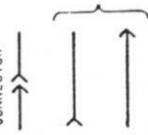


NON-STANDARD
VOLTAGE LEVELS

OUTPUT



CONNECTOR



UNUSED PINS



SYMBOL SIZE DETERMINED
BY NUMBER OF INPUTS OR OUTPUTS USED.

LOGIC STATE INDICATOR

LOGICAL 0 INPUT - THE PRESENCE OF A CIRCLE ON AN INPUT LINE INDICATES THAT THE LOGICAL 0 STATE IS REQUIRED TO PERFORM THE INDICATED LOGIC FUNCTION OF THE SYMBOL
LOGICAL 1 INPUT - THE ABSENCE OF A CIRCLE ON AN INPUT LINE INDICATES THAT THE LOGICAL 1 STATE IS REQUIRED TO PERFORM THE INDICATED LOGIC FUNCTION OF A SYMBOL
LOGICAL 0 OUTPUT - THE PRESENCE OF A CIRCLE ON AN OUTPUT LINE INDICATES THAT THE LOGIC FUNCTION HAS AN OUTPUT OF LOGICAL 0 WHEN THE FUNCTION IS SATISFIED
LOGICAL 1 OUTPUT - THE ABSENCE OF A CIRCLE ON AN OUTPUT LINE INDICATES THAT THE LOGIC FUNCTION HAS AN OUTPUT OF LOGICAL 1 WHEN THE FUNCTION IS SATISFIED

LOGIC LEVELS

DTL LOGIC OPERATION

HIGH (LOGICAL 1) = +2.6 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0 TO +0.45 VOLTS
SWITCHING POINT = +1.1 TO +1.9 VOLTS

TTL LOGIC OPERATION

HIGH (LOGICAL 1) = +2.8 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0V TO +0.45 VOLTS
SWITCHING POINT = +0.85V TO +1.9 VOLTS

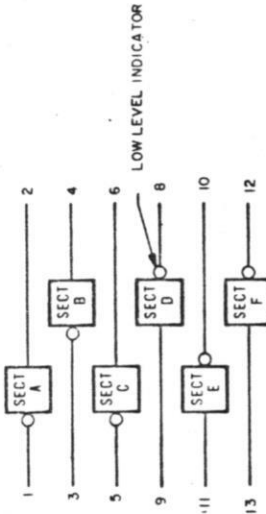
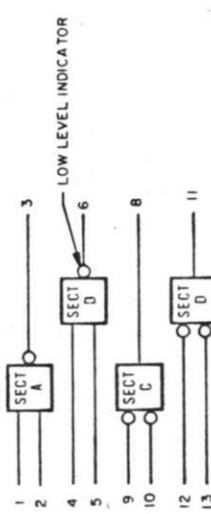
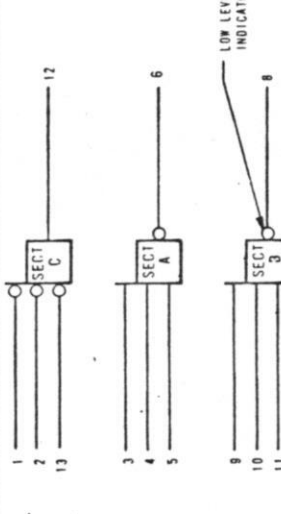
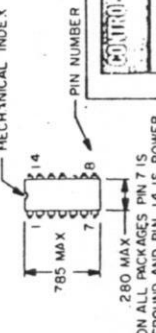
NOTE: AN UNUSED INPUT PIN ON AN INTEGRATED CIRCUIT IS CONSIDERED AT A LOGICAL 1 VOLTAGE LEVEL.

ABBREVIATIONS

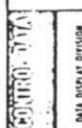
MEANINGS
L. INTEN = LINE INTENSITY
N. L. = NEW LINE
MUX = MULTIPLEX
MC = MASTER CLEAR
ROM = READ ONLY MEMORY
T. C. = TERMINAL COUNT
T. = TIME
X = HORIZONTAL
Y = VERTICAL

KEY TO SYMBOLS

CODE INPUT 15920
CROSS REF. NO. 62164300
SHEET 3

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT	PROPAGATION DELAY IN NANOSECONDS (SEE NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES																																								
129 HEX INVERTER GATES PN 51654400		1L 8L	$t_{pd}(+) = 25-80$ $t_{pd}(-) = 10-30$	1. THE OUTPUT IS THE COMPLEMENT OF THE INPUT AND IS LOW WHEN THE INPUT IS FLOATING	THE OUTPUTS OF INTEGRATED CIRCUIT (IC) 129 MAY BE TIED TOGETHER TO FORM THE WIRED "OR" FUNCTION. A FANOUT OF 100 MUST BE SUBTRACTED FOR EACH ADDED GATE.																																								
140 140H TTL QUAD 2-INPUT GATE ELEMENT PN 51651900 PN 39388900		1L 10L	$t_{pd}(+) = 3.0-20$ $t_{pd}(-) = 2.0-15$		1. EITHER LOGIC SYMBOL (NAND, NOR) MAY BE USED TO REPRESENT THESE CIRCUITS DEPENDING UPON THE FUNCTION OF THE CIRCUIT IN THE PARTICULAR APPLICATION 2. INTEGRATED CIRCUIT (IC) 140 MAY NOT BE OUTPUT "OR" ED.																																								
141 TRIPLE 3-INPUT GATE ELEMENT PN 51650700		1L .10L	7ns	<table><tr><th colspan="2">INPUTS</th><th colspan="2">OUTPUTS</th></tr><tr><th>1</th><th>2</th><th>13</th><th>12</th></tr><tr><td>H</td><td>H</td><td>H</td><td>L</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td></tr><tr><td>H</td><td>L</td><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td><td>H</td><td>H</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>L</td><td>H</td><td>L</td><td>L</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td></tr></table>	INPUTS		OUTPUTS		1	2	13	12	H	H	H	L	L	H	H	H	H	L	H	H	L	L	H	H	H	H	L	L	L	H	L	L	H	L	L	L	L	L	L	L	1. EITHER LOGIC SYMBOL (NAND, NOR) MAY BE USED TO REPRESENT THESE CIRCUITS DEPENDING UPON THE FUNCTION OF THE CIRCUIT IN THE PARTICULAR APPLICATION 2. INTEGRATED CIRCUIT (IC) 141 MAY NOT BE WIRE - "OR" ED. 3. DUAL IN LINE PACKAGE
INPUTS		OUTPUTS																																											
1	2	13	12																																										
H	H	H	L																																										
L	H	H	H																																										
H	L	H	H																																										
L	L	H	H																																										
H	H	L	L																																										
L	H	L	L																																										
H	L	L	L																																										
L	L	L	L																																										
GENERAL NOTES FOR ALL CIRCUIT TYPES																																													
4. AVERAGE PROPAGATION DELAY (t_{pd}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE [$t_{pd}(+)$] AND NEGATIVE [$t_{pd}(-)$] OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF +1.5V. HENCE, $t_{pd} = \frac{t_{pd}(+) + t_{pd}(-)}{2}$ 																																													
5. TYPICAL DUAL IN-LINE PACKAGE.  ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER																																													
3. A. FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL, HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED.																																													
1. $+4.5 < V_{cc} < +5.5$ VOLTS 2. (A) AMBIENT OPERATING TEMPERATURE 0°C TO $+75^{\circ}\text{C}$ (B) STORAGE TEMPERATURE -65°C TO $+150^{\circ}\text{C}$																																													
KEY TO SYMBOLS																																													
15920 C 62164300																																													
DWG. NO. 62164300																																													
REV. 4																																													

KEY TO SYMBOLS


 ON ALL PACKAGES PIN 7 IS
 GROUND AND PIN 14 IS POWER

 CON. INT. 15920
 DMC NO. 62164300
 REV. NO. 4

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGIC BREAKDOWN WHERE NECESSARY	UNIT LOAD (L) 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS (SEE GEN NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES																																																																																								
142 TTL MASTER- SLAVE TRIGGERED FLIP FLOP WITH DIRECT SET AND DIRECT CLEAR PN 50250800		MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT	10L JK 2L SD } 2.7L CD }	<table><tr><th colspan="4">SYNCHRONOUS</th><th colspan="4">ASYNCHRONOUS</th></tr><tr><th colspan="4">INPUTS</th><th colspan="4">INPUTS</th></tr><tr><td>J</td><td>K</td><td>Q</td><td>Q'</td><td>J</td><td>K</td><td>Q</td><td>Q'</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table> GROUND WHEN NOT IN USE AMBIGUOUS NO CHANGE HI LO TOGGLES	SYNCHRONOUS				ASYNCHRONOUS				INPUTS				INPUTS				J	K	Q	Q'	J	K	Q	Q'	0	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	1	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	1	1	0	1	1	1	0	THE "142" MAY BE USED EITHER AS AN R-S OR JK FLIP FLOP.
SYNCHRONOUS				ASYNCHRONOUS																																																																																									
INPUTS				INPUTS																																																																																									
J	K	Q	Q'	J	K	Q	Q'																																																																																						
0	0	0	1	0	0	0	1																																																																																						
0	1	0	1	0	1	0	1																																																																																						
1	0	0	1	1	0	0	1																																																																																						
1	1	0	1	1	1	0	1																																																																																						
0	0	1	0	0	0	1	0																																																																																						
0	1	1	0	0	1	1	0																																																																																						
1	0	1	0	1	0	1	0																																																																																						
1	1	1	0	1	1	1	0																																																																																						
143 TTL DUAL POWER GATE ELEMENT PN 51639900		1L 10L	1pd(+) = 30-20 1pd(-) = 20-15		1. EITHER LOGIC SYMBOL (NAND, NOR) MAY BE USED TO REPRESENT THESE CIRCUITS DEPENDING UPON THE FUNCTION OF THE CIRCUIT IN THE PARTICULAR APPLICATION. 2. INTEGRATED CIRCUIT (IC) 143 MAY NOT BE WIRE - "OR" ED.																																																																																								

GENERAL NOTES FOR ALL CIRCUIT TYPES					5 TYPICAL DUAL IN-LINE PACKAGE
1 -4.5 < V _{cc} < +5.5 VOLTS	4 AVERAGE PROPAGATION DELAY (t _{pd}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE (t _{pd(+)}) AND NEGATIVE (t _{pd(-)}) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF +1.5V HENCE t _{pd} = t _{pd(+)} + t _{pd(-)}	5 TYPICAL DUAL IN-LINE PACKAGE	TOP VIEW MECHANICAL INDEX 14 785 MAX PIN NUMBER 280 MAX ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER		
2 (A) AMBIENT OPERATING TEMPERATURE 0°C TO +70°C (B) STORAGE TEMPERATURE -65°C TO +150°C	3 A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL. HENCE UNUSED INPUTS MAY REMAIN UNCONNECTED				

KEY TO SYMBOLS		15920 C	62164300 A	15920 C	62164300 A
DATE DATA DIVISION		15920 C			

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGIC BREAKDOWN WHERE NECESSARY	UNIT LOGIC (L) 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS (SEE GEN. NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES																										
144 TTL MASTER-SLAVE TRIGGERED FLIP-FLOP WITH DIRECT SET AND DIRECT CLEAR PN 51623200		J } 1L K } CP } JK 2L SD } 2 7L CD }	10L $t_{pd}(+) = 20 \text{ MAX}$ $t_{pd}(-) = 30 \text{ MAX}$	SYNCHRONOUS INPUTS <table><tr><th>INPUTS</th><th>OUT-PUTS</th></tr><tr><td>J K J1 J2 J3 K1 K2 K3 Q Q</td><td>Q Q</td></tr><tr><td>L L L L L L L L</td><td>NC NC</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>T T</td></tr></table> ASYNCHRONOUS INPUTS OUTPUTS <table><tr><th>INPUTS</th><th>OUTPUTS</th></tr><tr><td>SD CD Q Q</td><td>Q Q</td></tr><tr><td>L L H H L L H H</td><td>NC NC</td></tr><tr><td>L L H H L L H H</td><td>L L</td></tr><tr><td>H L L L H L L L</td><td>L L</td></tr><tr><td>H H NC NC</td><td>T T</td></tr></table> Δ = GROUND WHEN NOT IN USE ? = AMBIGUOUS NC = NO CHANGE H = HI L = LO T = TOGGLES	INPUTS	OUT-PUTS	J K J1 J2 J3 K1 K2 K3 Q Q	Q Q	L L L L L L L L	NC NC	H H H H H H H H	L L	H H H H H H H H	L L	H H H H H H H H	L L	H H H H H H H H	T T	INPUTS	OUTPUTS	SD CD Q Q	Q Q	L L H H L L H H	NC NC	L L H H L L H H	L L	H L L L H L L L	L L	H H NC NC	T T	THE 144 MAY BE USED EITHER AS AN R-S OR JK FLIP FLOP.
INPUTS	OUT-PUTS																														
J K J1 J2 J3 K1 K2 K3 Q Q	Q Q																														
L L L L L L L L	NC NC																														
H H H H H H H H	L L																														
H H H H H H H H	L L																														
H H H H H H H H	L L																														
H H H H H H H H	T T																														
INPUTS	OUTPUTS																														
SD CD Q Q	Q Q																														
L L H H L L H H	NC NC																														
L L H H L L H H	L L																														
H L L L H L L L	L L																														
H H NC NC	T T																														
145 145H TTL DUAL 2-2 INPUT GATE ELEMENT PN 51701900 PN 39389000		1L 10L	$t_{pd}(+) = 3-15$ $t_{pd}(-) = 3-15$	1. THE ADDITION OF ONE OR MORE INTEGRATED CIRCUITS (IC) 144'S DOES NOT ALTER THE LOGICAL FUNCTION OF THE EXPANDED CIRCUIT AND THE GENERAL RULE REMAINS VALID. ANY COMBINATION OF ONE OR MORE LO INPUTS FORCES THE OUTPUT HI.	1. THE USE OF EXPANDERS DOES NOT EFFECT QUIESCENT LOADING OF THE INPUT-EXPANDED ELEMENT. HOWEVER, THE ADDED INPUT CAPACITANCE DECREASES NOISE IMMUNITY AND INCREASES t_{pd} . INPUTS MAY BE EXPANDED BY 20 WITHOUT ADVERSELY AFFECTING FANOUT CAPABILITY OR NOISE IMMUNITY IN THE EXPANDED ELEMENT. THE EXPANDER WIRING MUST BE KEPT SHORT AND WELL DRESSED TO MINIMIZE DISTRIBUTED CAPACITANCE. THE INTEGRATED CIRCUIT (IC) 145 HAS A TYPICAL $C_{IN} = 2 \text{ pF}$ AND $C_{OUT} = 5 \text{ pF}$.																										

GENERAL NOTES FOR ALL CIRCUIT TYPES					KEY TO SYMBOLS
5 TYPICAL DUAL IN-LINE PACKAGE TOP VIEW MECHANICAL INDEX 					
ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER					
4. AVERAGE PROPAGATION DELAY (t_{pd}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE ($t_{pd}(+)$) AND NEGATIVE ($t_{pd}(-)$) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF -1.5V. HENCE $t_{pd} = t_{pd}(+) + t_{pd}(-)$ 					
1. $+4.5 < V_{cc} < +5.5 \text{ VOLTS}$ 2. (A) AMBIENT OPERATING TEMPERATURE $0^\circ\text{C TO } +70^\circ\text{C}$ (B) STORAGE TEMPERATURE $-65^\circ\text{C TO } +150^\circ\text{C}$ 3. A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL. HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED					

LOGIC SYMBOL WITH APPLICATION OR LOGIC BREAKDOWN WHERE NECESSARY	UNIT LOGIC (L) 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS (SEE GEN. NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES																										
144 TTL MASTER-SLAVE TRIGGERED FLIP-FLOP WITH DIRECT SET AND DIRECT CLEAR PN 51623200	J } 1L K } CP } JK 2L SD } 2 7L CD }	10L $t_{pd}(+) = 20 \text{ MAX}$ $t_{pd}(-) = 30 \text{ MAX}$	SYNCHRONOUS INPUTS <table><tr><th>INPUTS</th><th>OUT-PUTS</th></tr><tr><td>J K J1 J2 J3 K1 K2 K3 Q Q</td><td>Q Q</td></tr><tr><td>L L L L L L L L</td><td>NC NC</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>L L</td></tr><tr><td>H H H H H H H H</td><td>T T</td></tr></table> ASYNCHRONOUS INPUTS OUTPUTS <table><tr><th>INPUTS</th><th>OUTPUTS</th></tr><tr><td>SD CD Q Q</td><td>Q Q</td></tr><tr><td>L L H H L L H H</td><td>NC NC</td></tr><tr><td>L L H H L L H H</td><td>L L</td></tr><tr><td>H L L L H L L L</td><td>L L</td></tr><tr><td>H H NC NC</td><td>T T</td></tr></table> Δ = GROUND WHEN NOT IN USE ? = AMBIGUOUS NC = NO CHANGE H = HI L = LO T = TOGGLES	INPUTS	OUT-PUTS	J K J1 J2 J3 K1 K2 K3 Q Q	Q Q	L L L L L L L L	NC NC	H H H H H H H H	L L	H H H H H H H H	L L	H H H H H H H H	L L	H H H H H H H H	T T	INPUTS	OUTPUTS	SD CD Q Q	Q Q	L L H H L L H H	NC NC	L L H H L L H H	L L	H L L L H L L L	L L	H H NC NC	T T	THE 144 MAY BE USED EITHER AS AN R-S OR JK FLIP FLOP.
INPUTS	OUT-PUTS																													
J K J1 J2 J3 K1 K2 K3 Q Q	Q Q																													
L L L L L L L L	NC NC																													
H H H H H H H H	L L																													
H H H H H H H H	L L																													
H H H H H H H H	L L																													
H H H H H H H H	T T																													
INPUTS	OUTPUTS																													
SD CD Q Q	Q Q																													
L L H H L L H H	NC NC																													
L L H H L L H H	L L																													
H L L L H L L L	L L																													
H H NC NC	T T																													
145 145H TTL DUAL 2-2 INPUT GATE ELEMENT PN 51701900 PN 39389000	1L 10L	$t_{pd}(+) = 3-15$ $t_{pd}(-) = 3-15$	1. THE ADDITION OF ONE OR MORE INTEGRATED CIRCUITS (IC) 144'S DOES NOT ALTER THE LOGICAL FUNCTION OF THE EXPANDED CIRCUIT AND THE GENERAL RULE REMAINS VALID. ANY COMBINATION OF ONE OR MORE LO INPUTS FORCES THE OUTPUT HI.	1. THE USE OF EXPANDERS DOES NOT EFFECT QUIESCENT LOADING OF THE INPUT-EXPANDED ELEMENT. HOWEVER, THE ADDED INPUT CAPACITANCE DECREASES NOISE IMMUNITY AND INCREASES t_{pd} . INPUTS MAY BE EXPANDED BY 20 WITHOUT ADVERSELY AFFECTING FANOUT CAPABILITY OR NOISE IMMUNITY IN THE EXPANDED ELEMENT. THE EXPANDER WIRING MUST BE KEPT SHORT AND WELL DRESSED TO MINIMIZE DISTRIBUTED CAPACITANCE. THE INTEGRATED CIRCUIT (IC) 145 HAS A TYPICAL $C_{IN} = 2 \text{ pF}$ AND $C_{OUT} = 5 \text{ pF}$.																										

GENERAL NOTES FOR ALL CIRCUIT TYPES					KEY TO SYMBOLS
5 TYPICAL DUAL IN-LINE PACKAGE TOP VIEW MECHANICAL INDEX 					
ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER					
4. AVERAGE PROPAGATION DELAY (t_{pd}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE ($t_{pd}(+)$) AND NEGATIVE ($t_{pd}(-)$) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF -1.5V. HENCE $t_{pd} = t_{pd}(+) + t_{pd}(-)$ 					
1. $+4.5 < V_{cc} < +5.5 \text{ VOLTS}$ 2. (A) AMBIENT OPERATING TEMPERATURE $0^\circ\text{C TO } +70^\circ\text{C}$ (B) STORAGE TEMPERATURE $-65^\circ\text{C TO } +150^\circ\text{C}$ 3. A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL. HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED					

5 TYPICAL DUAL IN-LINE PACKAGE

TOP VIEW

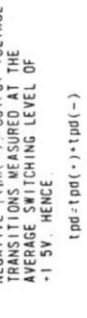
MECHANICAL INDEX



ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER

4. AVERAGE PROPAGATION DELAY (t_{pd}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE ($t_{pd}(+)$) AND NEGATIVE ($t_{pd}(-)$) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF -1.5V. HENCE:

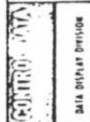
$t_{pd} = \frac{t_{pd}(+) + t_{pd}(-)}{2}$



GENERAL NOTES FOR ALL CIRCUIT TYPES

- $+4.5 < V_{cc} < +5.5 \text{ VOLTS}$
- (A) AMBIENT OPERATING TEMPERATURE $0^\circ\text{C TO } +70^\circ\text{C}$
(B) STORAGE TEMPERATURE $-65^\circ\text{C TO } +150^\circ\text{C}$
- A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL. HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED

KEY TO SYMBOLS



15920	C	62164300	A
15920	C	62164300	A
15920	C	62164300	A

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L)		PROPAGATION DELAY IN NANOSECONDS (SEE GEN NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES
		MIN INPUT LOAD EACH INPUT	MAX FANOUT EACH OUTPUT			
146 146H TTL HEX INVERTER GATE ELEMENT PN 51701800 PN 52335800		1L	10L	TPD(+) = 3-8 TPD(-) = 3-7		1. THE INTEGRATED CIRCUIT (IC) 146 OUTPUTS MAY BE CONNECTED TO FORM THE WIRED "OR" FUNCTION
147 147H TTL EIGHT INPUT NAND GATE PN 50251900 PN 51801400		1L	10L	7 ns		1. EITHER LOGIC SYMBOL (NAND, NOR) MAY BE USED TO REPRESENT THESE CIRCUITS DEPENDING UPON THE FUNCTION OF THE CIRCUIT IN THE PARTICULAR APPLICATION 2. THE 147 CIRCUIT IS AN ACTIVE LOW LEVEL OUTPUT "AND" GATE COMMONLY KNOWN AS A "NAND" GATE
GENERAL NOTES FOR ALL CIRCUIT TYPES 1. $-4.5 < V_{EE} < +5$ VOLTS 2. (A) AMBIENT OPERATION TEMPERATURE: 0°C TO +70°C (B) STORAGE TEMPERATURE: -65°C TO +150°C 3. A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HI INPUT SIGNAL. HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED 4. AVERAGE PROPAGATION DELAY (t_{PD}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE ($t_{PD}(+)$) AND NEGATIVE ($t_{PD}(-)$) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF +1.5V. HENCE: $t_{PD} = [t_{PD}(+) + t_{PD}(-)] / 2$ 5. TYPICAL DUAL IN-LINE PACKAGE ON ALL PACKAGES PIN 7 IS GROUND AND PIN 14 IS POWER						

CODE 14447	15920	DATE NO	C	62164300	REV	A
KEY TO SYMBOLS			PART NUMBER			SHEET 7

CIRCUIT TYPES	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) = 1.6 MA MAX MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
138 TTL UP BINARY COUNTER PN 51761500	PIN NAMES PE, P0, P1, P2, P3 CET, CET, CET, CET MR, Q0, Q1, Q2, Q3, TC PARALLEL ENABLE (ACTIVE LOW) INPUT PARALLEL INPUTS COUNT ENABLE PARALLEL INPUT COUNT ENABLE TRICKLE INPUT CLOCK ACTIVE HIGH GOING EDGE INPUT MASTER RESET (ACTIVE LOW) INPUT PARALLEL OUTPUTS TERMINAL COUNT OUTPUT	MIN INPUT LOAD EACH INPUT: 2L MAX FANOUT EACH OUTPUT: 6L TC = 6L CET = 1L CP = 2L MR = 1L	CP 18ns	1. THE 138 CXT IS A 4 BIT SYNCHRONOUS BINARY UP COUNTER. IT HAS SYNCHRONOUS PARALLEL LOAD FACILITY, OVERRIDING ASYNCHRONOUS MASTER RESET AND CARRY LOOKAHEAD LOGIC FOR HIGH SPEED MULTISTAGE OPERATION. 2. THE COUNTER IS SYNCHRONOUS. WITH THE COUNTER OUTPUTS CHANGING STATE AFTER THE LOW TO HIGH TRANSITION OF THE CLOCK. WHEN CONDITIONS ARE SATISFIED FOR COUNTING, A CLOCK PULSE WILL CHANGE THE COUNTER TO THE NEXT STATE OF BINARY SEQUENCE. WHEN THE PARALLEL ENABLE IS LOW THE PARALLEL INPUTS DETERMINE THE NEXT STATE OF THE COUNTER SYNCHRONOUSLY WITH THE CLOCK. 3. MODE SELECTION IS ACCOMPLISHED AS SHOWN BELOW. HOWEVER A RESTRICTION IS PLACED ON THE MANNER OF SELECTION. THE TRANSITION OF "CET" OR "CET" FROM HIGH TO LOW OR OF PE FROM LOW TO HIGH MAY ONLY BE DONE WHEN "CP" IS HIGH. BY UTILIZING THE TWO COUNTENABLE INPUTS AND TERMINAL COUNT OUTPUT MULTI-STAGE SYNCHRONOUS COUNTING IS OBTAINED. WITH OPERATING SPEEDS EQUIVALENT TO THAT OF A SINGLE STAGE. WHEN THE SYNCHRONOUS MASTER RESET IS ACTIVE OUTPUTS Q0-3 WILL BE FORCED LOW REGARDLESS OF ALL OTHER INPUT CONDITIONS.

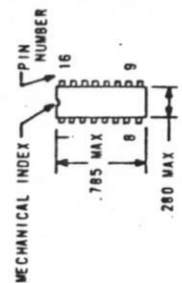
MODE SELECTION

PE	CE (COUNT ENABLE)	MODE
H	H	COUNT UP
H	L	NO CHANGE
L	X	PRESETTING

WHERE CE (COUNT ENABLE) = CET

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

TOP VIEW



LOGIC EQUATION FOR TERMINAL COUNT

$$T_C = C_{ET} \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$$

PIN 16 = V_{CC}
PIN 8 = GND

KEY TO SYMBOL 3

CODE 10411
15920

QWG NO
62164300

SHEET 8

CIRCUIT DESCRIPTION AND SPECIFIC NOTES

1. THE 159 CKT IS A SYNCHRONOUS 4-BIT SHIFT REGISTER DESIGNED TO PERFORM FUNCTIONS SUCH AS STORAGE, SHIFTING COUNTING AND SERIAL CODE CONVERSION. IT HAS ASSERTION OUTPUTS ON EACH STAGE AND A NEGATIVE OUTPUT ON THE LAST STAGE. AN OVERDRIVING ASYNCHRONOUS MASTER RESET, JK INPUT CONFIGURATION, AND A SYNCHRONOUS PARALLEL LOAD FACILITY.
2. DATA ENTRY IS SYNCHRONOUS WITH THE REGISTERS CHANGING STATE AFTER EACH LOW TO HIGH TRANSITION OF THE CLOCK. WITH THE PARALLEL ENABLE LOW THE PARALLEL INPUTS DETERMINE THE NEXT CONDITION OF THE SHIFT REGISTER. WHEN THE PARALLEL ENABLE INPUT IS HIGH THE SHIFT REGISTER PERFORMS A ONE-BIT SHIFT TO THE RIGHT. WITH DATA ENTERING THE FIRST STAGE FLIP-FLOP THROUGH JK INPUTS. BY TYPING THE TWO INPUTS TOGETHER D TYPE ENTRY IS OBTAINED.
3. THE ASYNCHRONOUS ACTIVE LOW MASTER RESET WHEN ACTIVATED OVERRIDES ALL OTHER INPUT CONDITIONS AND CLEARS THE REGISTER.
4. TYPICAL POWER DISSIPATION PER FUNCTION = 300 MW.

TRUTH TABLE FOR SERIAL ENTRY

J	K	Q _n AT t _n + 1
L	L	L
L	H	Q _n AT t _n (NO CHANGE)
H	L	Q _n AT t _n (TOGGLES)
H	H	H

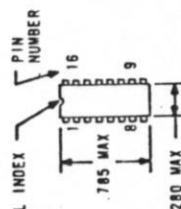
$\overline{PE}$ = HIGH

$\overline{WR}$ = HIGH

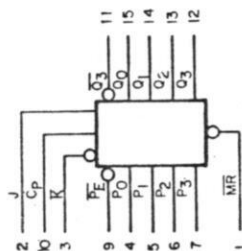
(n+1) = INDICATES STATE AFTER NEXT CLOCK

PIN 16 = V_{CC}
PIN 8 = GND

TOP VIEW



LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY



PIN NAMES

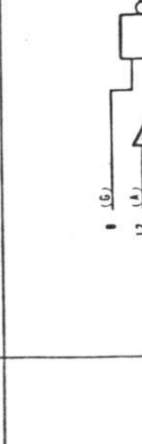
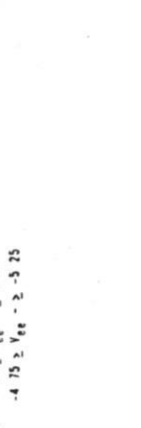
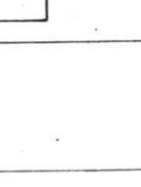
- $\overline{PE}$ PARALLEL ENABLE (ACTIVE LOW) INPUT
- P₀, P₁, P₂, P₃ PARALLEL INPUTS
- J FIRST STATE J (ACTIVE HIGH) INPUT
- K FIRST STATE K (ACTIVE LOW) INPUT
- CP CLOCK ACTIVE HIGH GOING EDGE INPUT
- $\overline{WR}$ MASTER RESET (ACTIVE LOW) INPUT
- Q₀, Q₁, Q₂, Q₃ PARALLEL OUTPUTS
- Q₃ COMPLEMENTARY LAST STAGE OUTPUT

159
TTL
4-BIT
UNIVERSAL
REGISTER
P/N
51754700

KEY TO SYMBOLS

DATE

REV	DWG NO	CRUIS	SHEET
1	62164300	15920	9

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (1) 1.5 MAX	MIN MAX INPUT LOAD EACH INPUT	PROPAGATION DELAY IN NANSECONDS (SEE GEN NOTE 3)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES															
162 DUAL IN-LINE RECEIVERS 50252900				8L	<table border="1"> <thead> <tr> <th>DIFF. INPUTS (A-B)</th> <th>STROBES</th> <th>OUTPUT (Y)</th> </tr> </thead> <tbody> <tr> <td>$V_{DD} \leq V_{in} \leq V_{DD}$</td> <td>L, L, L, L</td> <td>H, H, H, H</td> </tr> <tr> <td>$V_{DD} \leq V_{in} \leq V_{DD}$</td> <td>L, L, L, L</td> <td>L, L, L, L</td> </tr> <tr> <td>$V_{DD} \leq V_{in} \leq V_{DD}$</td> <td>L, L, L, L</td> <td>H, H, H, H</td> </tr> <tr> <td>$V_{DD} \leq V_{in} \leq V_{DD}$</td> <td>L, L, L, L</td> <td>L, L, L, L</td> </tr> </tbody> </table>	DIFF. INPUTS (A-B)	STROBES	OUTPUT (Y)	$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	H, H, H, H	$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	L, L, L, L	$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	H, H, H, H	$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	L, L, L, L	1 (A) AMBIENT OPERATING TEMPERATURE 0°C TO +70°C 1 (B) STORAGE TEMPERATURE -65°C TO +150°C 2 $4.75 \leq V_{EE} \leq 5.25$ -4.75 $\leq V_{EE} \leq -5.25$ 3 DUAL IN-LINE PACKAGE TOP VIEW  PIN 7 = GND PIN 13 = -5V PIN 14 = +5V
DIFF. INPUTS (A-B)	STROBES	OUTPUT (Y)																			
$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	H, H, H, H																			
$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	L, L, L, L																			
$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	H, H, H, H																			
$V_{DD} \leq V_{in} \leq V_{DD}$	L, L, L, L	L, L, L, L																			
LOGIC SYMBOL																					
GENERAL NOTES FOR ALL CIRCUIT TYPES	1 -4.5 $\leq V_{EE} \leq +5$ VOLTS 2 A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HIGH INPUT SIGNAL. HENCE, UNUSED INPUTS MAY REMAIN UNCONNECTED	3 AVERAGE PROPAGATION DELAY (T_{PD}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE AND NEGATIVE T_{PD} OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF +1.5V HENCE																			

KEY TO SYMBOLS

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CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	UNIT LOADS = 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
167 DTL ONE OF SIXTEEN DECODER PN 51754800	PIN NAMES A₀, A₁, A₂, A₃ E₀, E₁ Y₀ TO Y₁₅ ADDRESS INPUTS "AND" ENABLE (ACTIVE LOW) INPUTS (ACTIVE LOW) OUTPUTS	MIN INPUT LOAD EACH MAX FANOUT EACH OUTPUT	A TO OUTPUT } 21ns E TO OUTPUT } 17ns	1. THE 167 ONE OF SIXTEEN DECODER ACCEPTS FOUR BINARY WEIGHTED INPUTS AND PROVIDES ONE LOW OUTPUT CORRESPONDING TO THE INPUT CODE. 2. BOTH ENABLE INPUTS MUST BE LOW FOR ANY OUTPUT TO BE LOW. THE ACTIVE LOW OUTPUTS AND "AND" GATE ENABLING MAKES THE "167" SUITABLE FOR MEMORY AND CONTROL DECODING AND DEMULTIPLEXING APPLICATIONS. 3. THE 167 CAN DEMULTIPLEX DATA BY ROUTING IT FROM ONE INPUT TO ONE OF SIXTEEN POSSIBLE DECODER OUTPUTS. THE DESIRED OUTPUT IS ADDRESSED AND THE DATA IS APPLIED TO ONE OF THE ENABLE INPUTS. PROVIDING THAT THE OTHER ENABLE IS LOW, THE ADDRESSED OUTPUT WILL FOLLOW THE STATE OF THE APPLIED DATA. 4. TYPICAL POWER DISSIPATION PER FUNCTION = 175 MW

CONTROL DATE:	KEY TO SYMBOLS	CODE REPORT C	DWG NO 62164300	SHEET 12
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CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 DRIVE UNIT 2 MIN 3 MAX 4 INPUT 5 LOAD 6 EACH 7 INPUT 8 OUTPUT	PROPAGATION DELAY IN NANOSECONDS (SEE GEN. NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR THE INDIVIDUAL CIRCUIT TYPES																																																																																																
176 DUAL DIFFERENTIAL LINE DRIVER PIN 50252800		PINS 1 2 3 4 5 6 = 100 PIN 10 = 200	15 ns MAX FROM INPUT A OR B TO OUTPUTS Y OR Z	<table border="1"> <thead> <tr> <th colspan="2">LOGIC INPUTS</th> <th colspan="2">INITIATION INPUTS</th> <th colspan="2">OUTPUTS</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> </tbody> </table> NOTE LOW OUTPUT REPRESENTS THE ON STATE HIGH OUTPUT REPRESENTS THE OFF STATE	LOGIC INPUTS		INITIATION INPUTS		OUTPUTS		A	B	C	D	Y	Z	L	L	L	L	H	H	L	L	L	H	L	L	L	H	L	L	L	L	L	H	L	H	L	H	L	L	H	L	L	L	L	L	H	H	L	H	L	H	H	L	L	L	L	H	H	H	L	H	H	L	L	L	L	L	H	L	L	H	L	H	H	H	L	L	L	L	H	H	L	H	L	H	H	H	H	L	L	L	H	H	H	H	L	H	1 THE 176 ACCEPTS A DTL OR TTL LOGIC SIGNAL AND TRANSMITS IT OVER A DIFFERENTIAL LINE PAIR 2 ON STATE OUTPUT CURRENT IS 8 mA TO 15 mA 3 4 75 Vcc 5 25 -4 75 Vcc -5 25 4 DUAL IN LINE PACKAGE TOP VIEW MECHANICAL INDEX PIN 7 GROUND
LOGIC INPUTS		INITIATION INPUTS		OUTPUTS																																																																																																	
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GENERAL NOTES FOR ALL CIRCUIT TYPES	4 AVERAGE PROPAGATION DELAY (T _{PD}) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE (t _{PH}) AND NEGATIVE (t _{PL}) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL OF ±1.5V HENCE $T_{PD} = \frac{t_{PH} + t_{PL}}{2}$																																																																																																				
1 -4.5 V _{cc} +5.5 VOLTS 2 (A) AMBIENT OPERATION TEMPERATURE 0° C TO +75° C (B) STORAGE TEMPERATURE -65° C TO +150° C 3 A FLOATING (UNCONNECTED) INPUT IS THE LOGICAL EQUIVALENT OF A HIGH INPUT SIGNAL. HENCE UNUSED INPUTS MAY REMAIN UNCONNECTED																																																																																																					

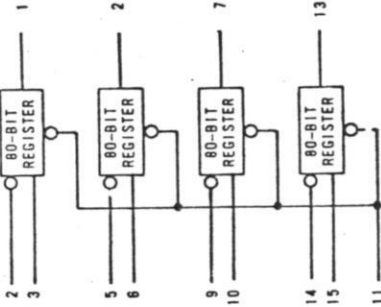
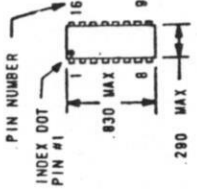
KEY TO SYMBOLS

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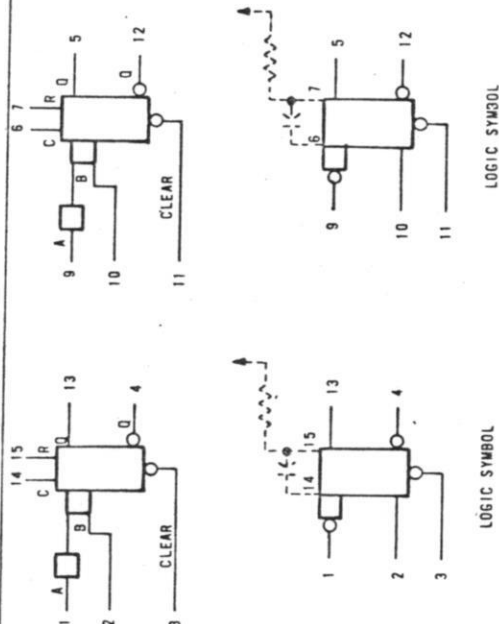
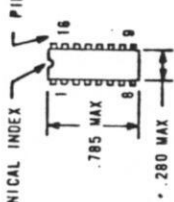
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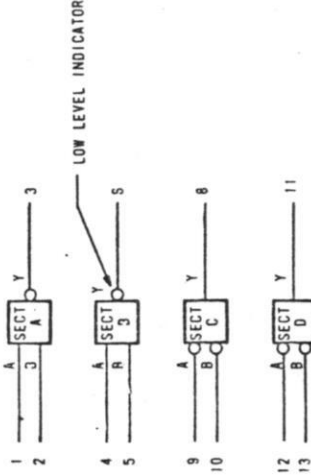
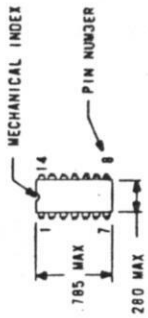
CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) = 1.6 x 10 ⁻¹² F	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
183 QUAD 80-BIT MOS SHIFT REGISTER P/N 51768300		MIN INPUT LOAD EACH INPUT 2 } = 1L 5 } 9 } 14 } 3 } 6 } = 1L 10 } 15 } 11 = 4L	NOT APPLICABLE	1. THE "183" IS A QUAD 80 BIT MOS DYNAMIC SHIFT REGISTER CAPABLE OF TEMPORARILY STORING BINARY DATA IN NRZ FORM. EACH OF THE FOUR 80-BIT SHIFT REGISTERS HAS ITS OWN RECIRCULATE ENABLE. DATA INPUT, DATA OUTPUT WITH ALL REGISTERS SHARING A COMMON CLOCK INPUT. A DYNAMIC CLOCK INPUT (PIN 11) KEEPS THE DATA IN CONSTANT RECIRCULATION WITHIN THE 80 BIT SHIFT REGISTER. 2. THE RECIRCULATE ENABLE AT A LOGICAL "1" WILL KEEP PREVIOUSLY ENTERED DATA RECIRCULATING AND AVAILABLE AT THE OUTPUT. 3. WHEN THE RECIRCULATE ENABLE IS SET TO "0" THE DATA AVAILABLE AT THE DATA INPUT WILL BE ENTERED INTO THE SHIFT REGISTER DURING THE POSITIVE PORTION OF THE CLOCK. THIS NEW DATA WILL BE AVAILABLE AT THE OUTPUT (80 X CLOCK CYCLE TIME IN MICROSECONDS) MICROSECONDS LATER THE RECIRCULATE ENABLE IS SET TO "0" ONLY FOR THE TIME REQUIRED TO CHANGE THE DESIRED BITS IN THE SHIFT REGISTER. 4. TYPICAL POWER DISSIPATION PER FUNCTION = 330 MW. VOLTAGES V_{SS} = PIN 16 = +5V V_{GG} = PIN 12 = -12V V_{DD} = PIN 8 = 0V TOP VIEW 

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	UNIT LOAD (L) 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
187 QUAD EXCLUSIVE OR GATE P/N 51783800		MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT 4 5 6 7 11 12 10 9 1 2 3 14 15 10L 13 (PINS 6 AND 10 HAVE AN OUTPUT DRIVE CAPABILITY OF 9)	12 ns	1. THE 187TH CKT CONSISTS OF FOUR 2 INPUT EXCLUSIVE "OR" GATES WHICH PRODUCE A HIGH OUTPUT WHEN THE INPUTS ARE COMPLEMENTARY. TWO OF THE GATES HAVE AN ADDITIONAL INVERTED OUTPUT WHICH PROVIDES A COMPARE CAPABILITY. TYPICAL POWER DISSIPATION PER FUNCTION = 25 mW PIN 16 = V_{CC} PIN 8 = GND TOP VIEW
191 ONE OF TEN DECODER P/N 95305700		MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT A₀ A₁ A₂ A₃ 10L 9	A TO 22ns OUTPUT	1. THE 191TH CKT ACCEPTS FOUR BINARY WEIGHTED INPUTS AND PROVIDES ONE OF TEN MUTUALLY EXCLUSIVE ACTIVE LOW OUTPUTS. WHEN A BINARY CODE GREATER THAN 9 IS APPLIED, ALL OUTPUTS ARE HIGH. THIS FACILITATES BCD TO DECIMAL CONVERSIONS AND EIGHT CHANNEL DEMULTIPLEXING AND DECODING. THE ACTIVE LOW DECODER OUTPUTS ARE COMPATIBLE WITH THE LOW ENABLES OF OTHER MSI ELEMENT MAKING THE 191TH CKT USEFUL IN LOGIC SELECTION SCHEMES. 2. THE 191TH CKT CAN SERVE AS A ONE OF EIGHT DECODER WITH AN ACTIVE LOW ENABLE. THE A₃ INPUT ACTING AS THE ACTIVE LOW ENABLE. EIGHT CHANNEL DEMULTIPLEXING RESULTS WHEN DATA IS APPLIED TO THE A₃ INPUT AND THE DESIRED OUTPUT IS ADDRESSED BY A₀, A₁, A₂. 3. TYPICAL POWER DISSIPATION PER FUNCTION = 145 mW H = HIGH VOLTAGE LEVEL L = LOW VOLTAGE LEVEL PIN 16 = V_{CC} PIN 8 = GND TOP VIEW

KEY TO SYMBOLS	REV C 62164300 A	ENC NO 15920	CROSS REF NO	SHEET 15
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CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) 1.5 V _{OL} V _{OL}		PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES																																								
		MIN INPUT LOAD EACH INPUT	MAX FANOUT OUTPUT																																										
193 DUAL- RETRIGGERABLE MONOSTABLE MULTI- VIBRATORS WITH CLEAR PN 15105100	 LOGIC SYMBOL			21ns	TRUTH TABLE <table><tr><th colspan="2">INPUTS</th><th colspan="2">OUTPUTS</th></tr><tr><th>A</th><th>B</th><th>H</th><th>L</th></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td></tr><tr><td>L</td><td>H</td><td>L</td><td>L</td></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td></tr><tr><td>L</td><td>H</td><td>L</td><td>L</td></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td></tr></table> NOTES 1. t_n = TIME BEFORE INPUT TRANSITION 2. t_{n+1} = TIME AFTER INPUT TRANSITION 3. H = HIGH LEVEL INPUT, L = LOW LEVEL INPUT THESE MONOLITHIC TTL DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS FEATURE D-C TRIGGERING FROM HIGH-LEVEL AND LOW-LEVEL ACTIVE INPUTS, AND ALSO PROVIDE AN OVERRIDING DIRECT CLEAR INPUT. THE RETRIGGER CAPABILITY SIMPLIFIES THE GENERATION OF EXTREMELY LONG DURATION OUTPUT PULSES. SUCCESSIVE TRIGGERING INPUTS, HAVING A PERIOD SHORTER THAN THE DELAY TIME, PRODUCE A CONSTANT OUTPUT PULSE. THE OVERRIDING CLEAR CAPABILITY PERMITS ANY OUTPUT TO BE TERMINATED AT A PREDETERMINED TIME. TOP VIEW MECHANICAL INDEX  PIN 16 = V_{CC} PIN 8 = GND	INPUTS		OUTPUTS		A	B	H	L	H	H	H	H	H	L	L	L	L	H	L	L	L	L	L	L	H	H	L	L	H	L	L	L	L	H	L	L	L	L	L	L
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KEY TO SYMBOLS	15920	C	62164300	A
PART 17				

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) LOGIC SYMBOL MIN INPUT LOAD EACH INPUT MAX FANOUT EACH OUTPUT	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
201 QUADRUPLE 2-INPUT POSITIVE AND GATE PN 5601200				THE 201, WITH TOTEM-POLE OUTPUTS, DRIVES 10 NORMALIZED LOADS AT THE LOW OUTPUT LEVEL AND 20 LOADS AT THE HIGH OUTPUT LEVEL THE 201 IS CHARACTERIZED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE FROM 0°C TO 70°C TYPICAL DUAL-IN-LINE PACKAGE TOP VIEW  PIN 7 = GROUND PIN 14 = POWER

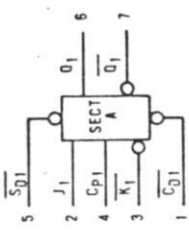
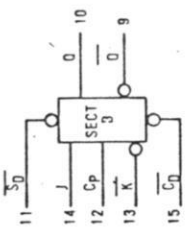
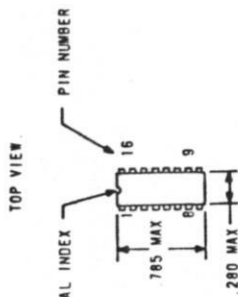
CONTROL DATE

KEY TO SYMBOLS

CODE REPORT
15920

ENG NO
62164300

SHEET 18

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) = 1.6 MA MAX		PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES																								
		MIN INPUT LOAD EACH INPUT	MAX ENOUT LOAD EACH OUTPUT																										
240 TTL DUAL J-K FLIP-FLOP P/N 51786700	 				1. THE "240" CKT HAS A MASTER SLAVE "JK" DESIGN, A HIGH SPEED AND HIGH NOISE IMMUNITY 2. THE MASTER SLAVE DESIGN OFFERS THE ADVANTAGE OF A "DC" THRESHOLD ON THE CLOCK INPUT INITIATING THE TRANSITION OF THE OUTPUTS SO THAT CAREFUL CONTROL OF CLOCK PULSE RISE AND FALL TIMES IS NOT REQUIRED 3. THE FLIP-FLOPS, WITH THE EXCEPTION OF A "142" CKT, HAVE J AND K INPUTS WHICH ALLOW D FLIP-FLOP OPERATION BY SIMPLY CONNECTING THE J AND K PIN TOGETHER 4. EACH FLIP-FLOP HAS ASYNCHRONOUS INPUTS WHICH PROVIDE THE ABILITY TO CONTROL THE STATE OF THE FLIP-FLOP INDEPENDENT STATIC CONDITIONS OF THE CLOCK AND ASYNCHRONOUS INPUTS BOTH ASYNCHRONOUS SET AND CLEAR IS PROVIDED ASYNCHRONOUS OPERATION <table><tr><th colspan="2">INPUTS</th><th colspan="2">OUTPUTS</th></tr><tr><td>S_D</td><td>C₀</td><td>Q</td><td>Q̄</td></tr><tr><td>L</td><td>L</td><td>H</td><td>H</td></tr><tr><td>L</td><td>H</td><td>H</td><td>L</td></tr><tr><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td></tr></table> TOP VIEW  PIN 8 = GND PIN 16 = VCC	INPUTS		OUTPUTS		S _D	C ₀	Q	Q̄	L	L	H	H	L	H	H	L	H	L	L	H	H	H	L	L
INPUTS		OUTPUTS																											
S _D	C ₀	Q	Q̄																										
L	L	H	H																										
L	H	H	L																										
H	L	L	H																										
H	H	L	L																										

KEY TO SYMBOLS		15920	C	62164300	REV. 19
				DEC NO	
				PROJ	
				PIN NC	

C	15920	62164300	A
C	15920	62164300	A
C	15920	62164300	A

KEY TO SYMBOLS

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	1 UNIT LOAD (L) = 1.6 MA MAX	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
500 TTL UP DOWN 4 BIT BINARY COUNTER P/N 36188600	9 DATA INPUT 23 10 DATA INPUT 22 1 DATA INPUT 21 15 DATA INPUT 20 4 COUNT DOWN 11 LOAD 13 COUNT UP 5 MASTER CLEAR 14 9 DATA OUTPUT 23 10 DATA OUTPUT 22 1 DATA OUTPUT 21 2 DATA OUTPUT 20 3 BORROW 13 CARRY 12 LOW-TO-HIGH LEVEL CARRY OUTPUT FROM COUNTUP INPUT HIGH-TO-LOW LEVEL CARRY OUTPUT FROM COUNTDOWN INPUT LOW-TO-HIGH LEVEL BORROW OUTPUT FROM COUNTDOWN INPUT HIGH-TO-LOW LEVEL BORROW OUTPUT FROM COUNTDOWN INPUT LOW-TO-HIGH LEVEL DATA OUTPUT FROM EITHER COUNT INPUT HIGH-TO-LOW LEVEL DATA OUTPUT FROM EITHER COUNT INPUT	MIN INPUT LOAD EACH INPUT 1 L MAX FANOUT EACH OUTPUT 10 L	17 16 16 16 25 31	1. THE 500 IS A MONOLITHIC SYNCHRONOUS 4 BIT BINARY UP/DOWN COUNTER HAVING THE NECESSARY CARRY AND BORROW OUTPUTS FOR CASCADED THE UP AND DOWN COUNTS TO HIGHER ORDER STAGES. 2. THE COUNT APPEARS AT THE DATA OUTPUTS TYPICALLY 31 ns AFTER THE NEGATIVE TRANSITION OF THE COUNT UP/DOWN INPUT. 3. BESIDES COUNTING UP AND DOWN FROM 0 - 17 THE COUNTER MAY ALSO BE PRESET TO ANY VALUE BY PRESENTING THE DESIRED DATA LEVELS AT THE DATA INPUTS AT LEAST 20 ns BEFORE THE LOAD PULSE. MASTER CLEAR UNCONDITIONALLY SETS THE DATA OUTPUTS TO "0". PIN 16 = V_{CC} PIN 8 = GND

DATE	KEY TO SYMBOLS	C 62164300	REV A
	15920	C 62164300	SHEET 20

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHEN NECESSARY	1 DRIVE UNIT (OUT) x 14 x 1 MAX MIN INPUT LOAD EACH INPUT	MIN FANOUT EACH OUTPUT	PROPAGATION DELAY IN NANoseconds (SEE GEN NOTE 4)	LOGIC OPERATION	SPECIFIC NOTES FOR INDIVIDUAL CIRCUIT TYPES
501 5 BIT COMPARATOR P.N. 51783500						THE 501 IS A HIGH SPEED EXPANDABLE COMPARATOR WHICH PROVIDES COMPARISON BETWEEN TWO FIVE BIT WORDS AND GIVES THREE OUTPUTS. LESS THAN, GREATER THAN AND EQUAL TO. A HIGH LEVEL ON THE ACTIVE LOW ENABLE INPUT FORCES ALL THREE OUTPUTS LOW. WORDS OF MORE THAN 5 BITS MAY BE COMPARED BY EITHER CONNECTING 501 COMPARATORS IN SERIES, OR BY CONNECTING COMPARATORS IN PARALLEL, AND COMPARING THE OUTPUTS WITH ANOTHER 501.
GENERAL NOTES FOR ALL CIRCUIT TYPES	1. $+4.5 < V_{EE} < +5.5$ VOLTS 2. (A) AMBIENT OPERATING TEMPERATURE 0°C TP $+75^{\circ}\text{C}$ (B) STORAGE TEMPERATURE -65°C TP $+150^{\circ}\text{C}$ 3. AVERAGE PROPAGATION DELAY (tpd) IS TAKEN AS THE MEAN DELAY OF BOTH THE POSITIVE (tpd(+)) AND NEGATIVE (tpd(-)) OUTPUT VOLTAGE TRANSITIONS MEASURED AT THE AVERAGE SWITCHING LEVEL $+1.5V$ HENCE, $tpd = tpd(+) + tpd(-)$					

KEY TO SYMBOLS

REV A

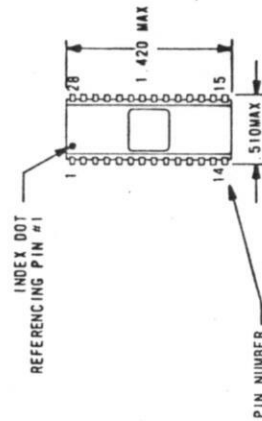
DWG NO 62164300

CODE IDENT 15920

CROSS SHEET 21

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	UNIT LOAD (L)		PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
		MIN INPUT LOAD EACH INPUT	MAX FANOUT EACH OUTPUT		
100 MOS 250W ROM 10 READ ONLY MEMORY P/N 51771400 51771401	OUTPUT WORD 18 6 A0 B0 5 A1 B1 7 A2 B2 14 A3 B3 11 A4 B4 10 A5 B5 9 A6 B6 8 A7 B7 16 CHIP ENABLE CE B8 15 READ IN RI B9 13 READ MEMORY RM V_{SS1} = PIN 1 = +5V V_{SS2} = PIN 3 = -12V V_{GG1} = PIN 2 = +5V V_{GG2} = PIN 4 = -12V V_{DD1} = PIN 17 = GND V_{DD2} = PIN 12 = GND V_{BB} = PIN 23 = GND PIN NAMES A0, A1, A2, A3, A4, A5, A6, A7 = ADDRESS INPUTS R1, RM = CLOCK INPUTS CE = CHIP ENABLE B0, B1, B2, B3, B4, B5, B6, B7, B8, B9 = OUTPUT WORD A0 ADDRESS INPUT 20 A1 ADDRESS INPUT 21 A2 ADDRESS INPUT 22 A3 ADDRESS INPUT 23 A4 ADDRESS INPUT 24 A5 ADDRESS INPUT 25 A6 ADDRESS INPUT 26 A7 ADDRESS INPUT 27	1L 1L	1L 1L	INTERNAL PROPAGATION DELAY IS 400ns DURING THE MINIMUM 600ns ACCESS TIME	1. READ ONLY MEMORIES 51771400 AND 51771401 ARE 256 WORD MEMORIES CONTAINING 10 BITS OF DATA AT EACH LOCATION. WITH THE DESIRED MEMORY ADDRESS PRESENT AT THE ADDRESS INPUTS, THE ADDRESS IS READ INTO THE ADDRESS REGISTER OF THE ROM BY THE NEGATIVE TRANSITION OF THE "READ IN" PULSE WITH CHIP ENABLE AT LOGICAL "1". THE CONTENTS OF THAT MEMORY LOCATION WILL APPEAR AT THE OUTPUT WORD NOT LATER THAN 400ns AFTER THE POSITIVE TRANSITION OF THE "READ MEMORY" PULSE. 2. CHIP ENABLE AT A LOGICAL "0" CAUSES THE OUTPUT WORD TO GO INTO AN INFINITE IMPEDANCE STATE.

TOP VIEW

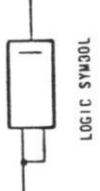
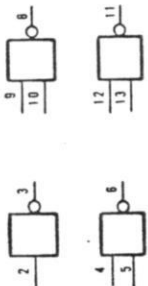
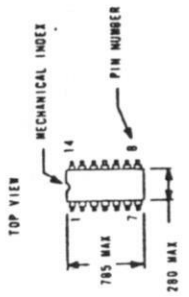
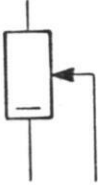
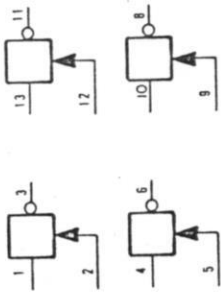
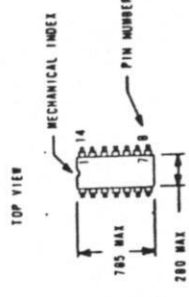


IN ITS USE AS A CHARACTER GENERATOR FOR RASTER SCAN DISPLAYS THE 10 BIT OUTPUT WORD IS USED IN 5 BIT BYTES TO WRITE ANY OF 5 HORIZONTAL DOTS IN THE 5 X 7 DOT MATRIX.

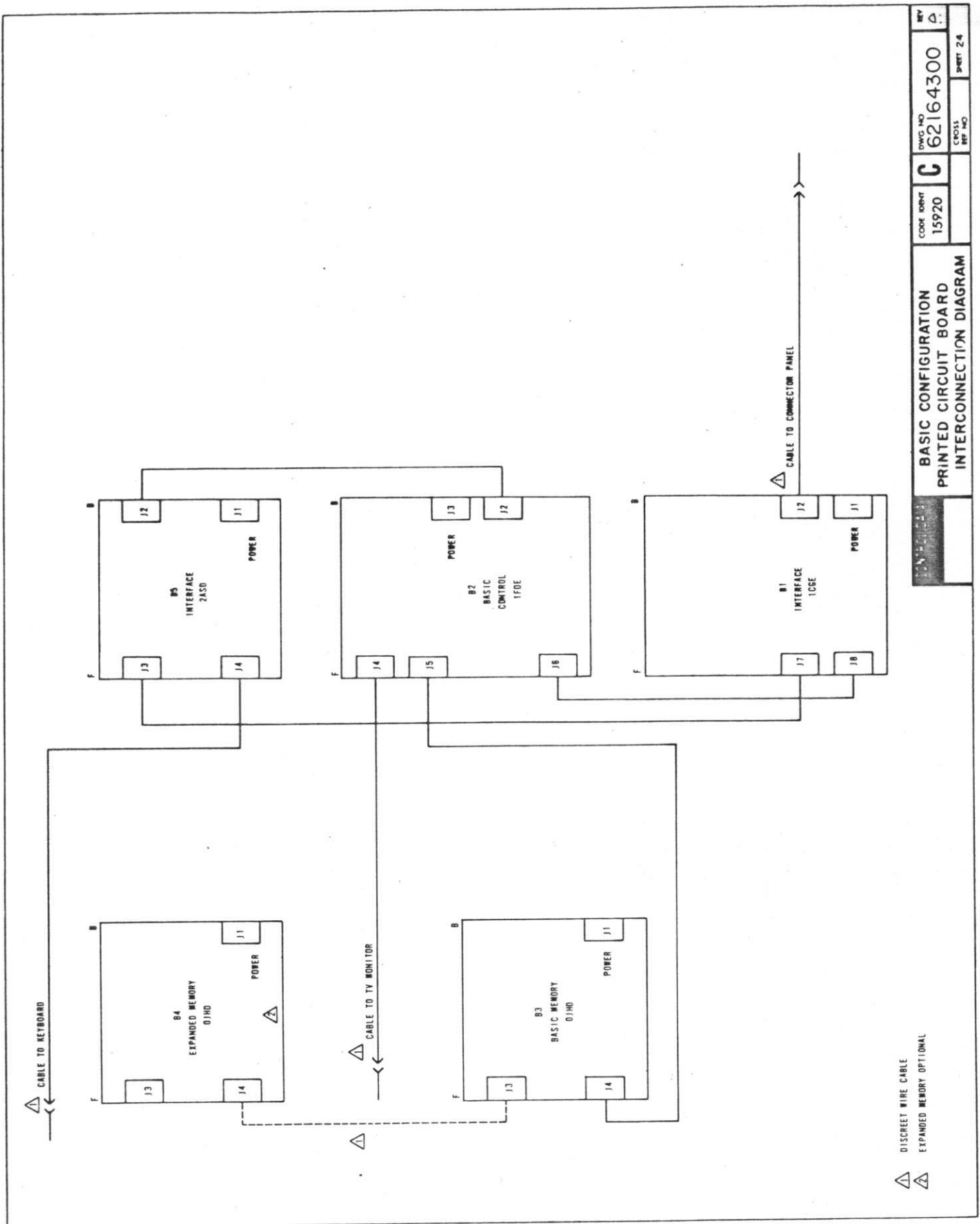
CONTINUED

KEY TO SYMBOLS

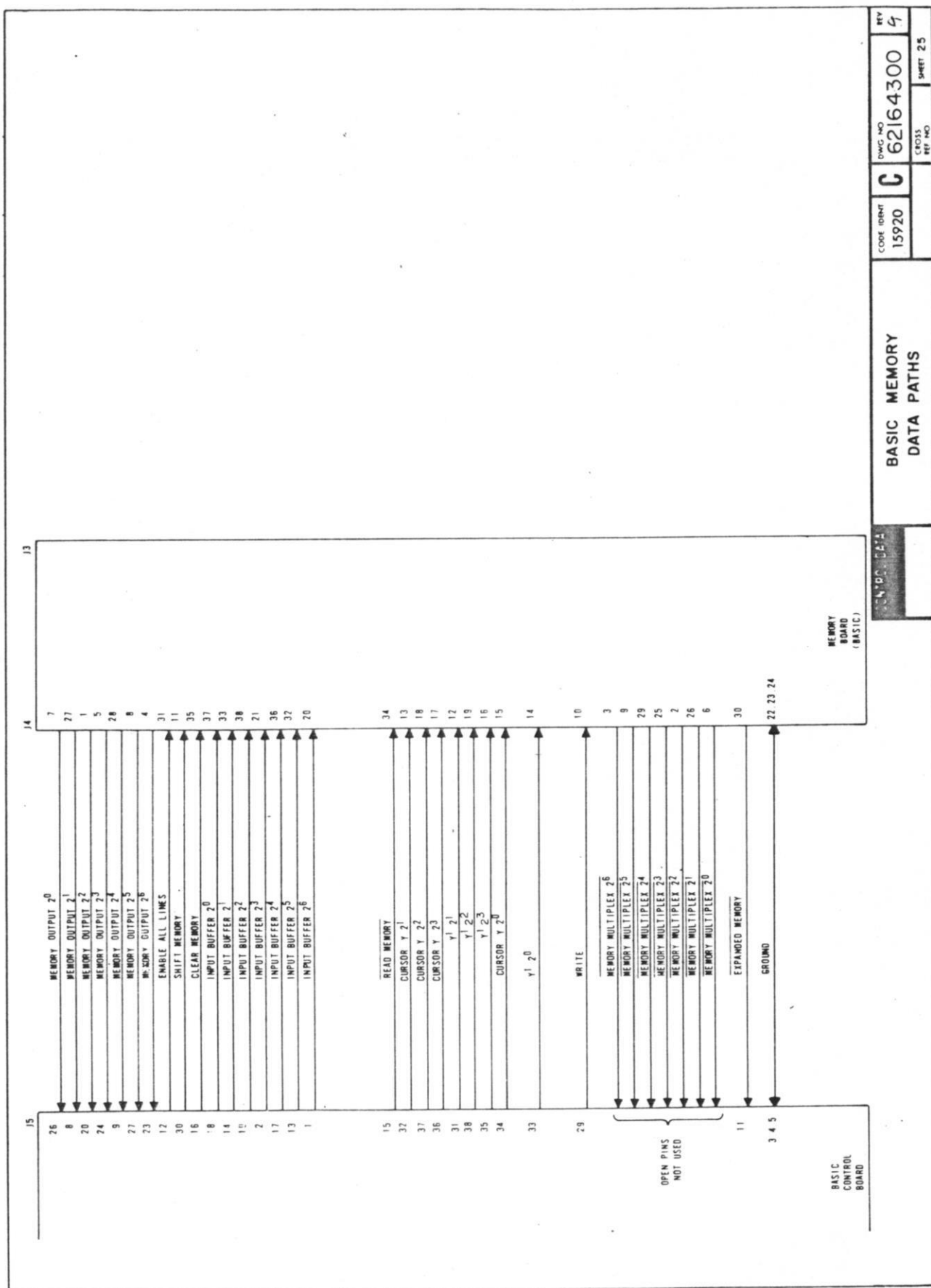
CODE IDENT	DWG NO	REV
15920	C 62164300	A
	CROSS REF NO	SHEET 22

CIRCUIT TYPE	LOGIC SYMBOL WITH APPLICATION OR LOGICAL BREAKDOWN WHERE NECESSARY	MIN. LOAD RES. FOLLOWS LOAD RES. FOLLOWS INPUT	PROPAGATION DELAY IN NANOSECONDS	CIRCUIT DESCRIPTION AND SPECIFIC NOTES
900 QUAD LINE DRIVER PN 38186400	 			THE 900 IS A MONOLITHIC QUAD LINE DRIVER DESIGNED TO INTERFACE DATA TERMINAL EQUIPMENT WITH DATA COMMUNICATIONS EQUIPMENT  PIN 7 = GND PIN 14 = $-V_{CC}$ PIN 1 = $-V_{CC}$
901 QUAD LINE RECEIVERS PN 36186500	 			THE 901 MONOLITHIC QUAD LINE RECEIVERS ARE DESIGNED TO INTERFACE DATA TERMINAL EQUIPMENT WITH DATA COMMUNICATIONS EQUIPMENT  PIN 7 = GND PIN 14 = V_{CC}

KEY TO SYMBOLS	C 62164300	15920	C 62164300	REV 1	PART 23
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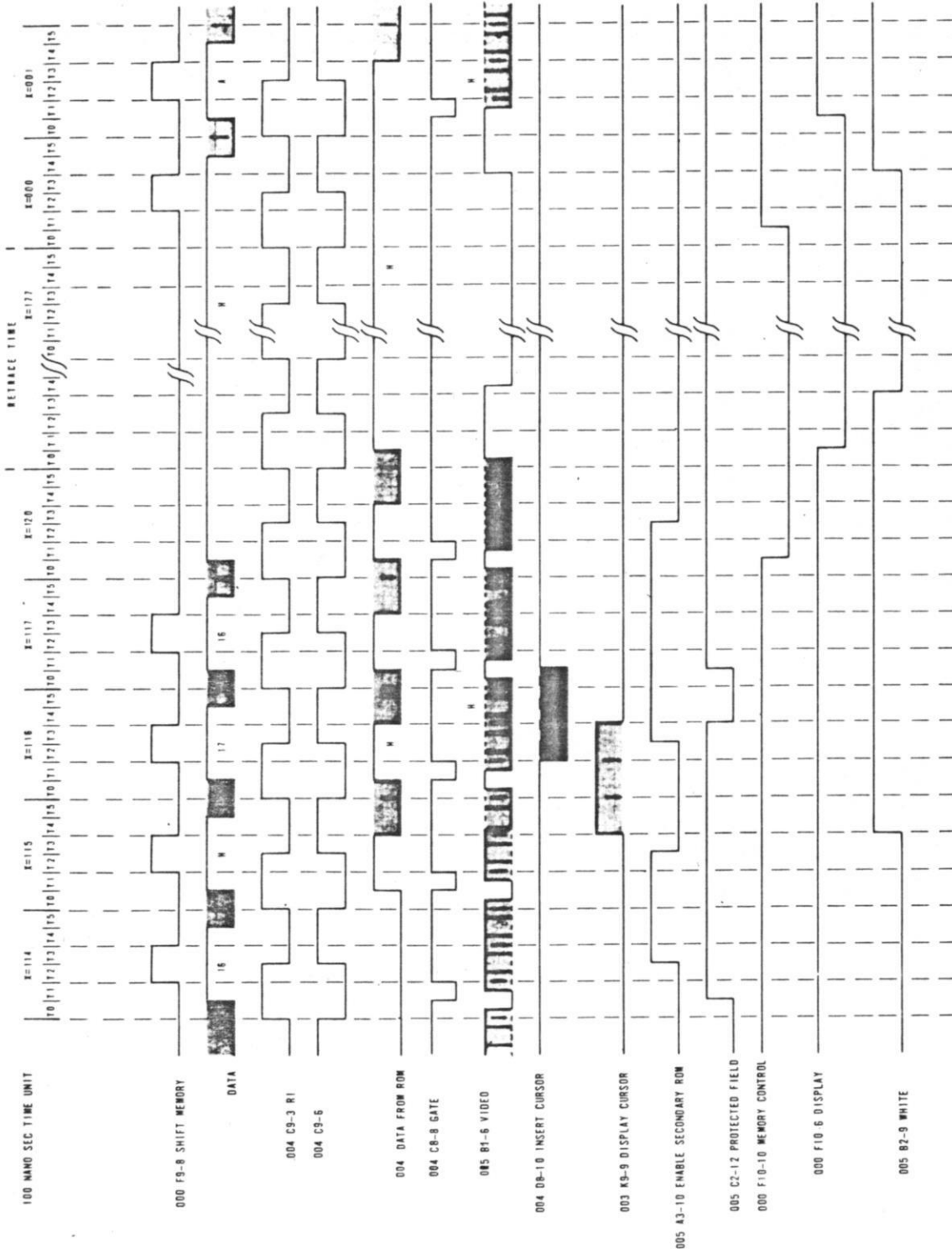


BASIC CONFIGURATION PRINTED CIRCUIT BOARD INTERCONNECTION DIAGRAM		CODE IDENT 15920	DOC NO 62164300	CROSS REF NO	SHEET 2-4
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BASIC MEMORY DATA PATHS		DWG. NO.	REV.
C		62164300	4
CODE IDENT	CROSS REF. NO.	SHEET 25	
15920			

100 NANO SEC TIME UNIT

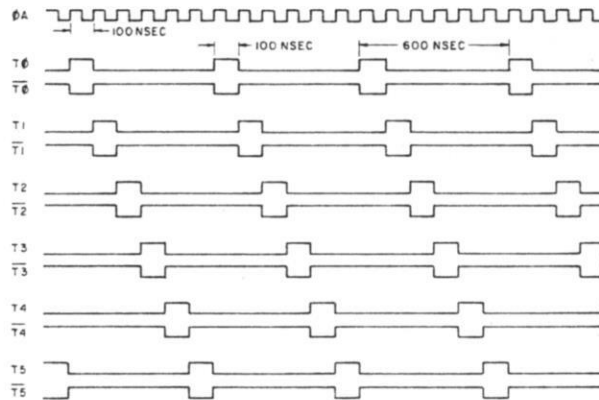


NOTE
SHADED AREAS INDICATE
INDETERMINABLE LOGIC
LEVELS

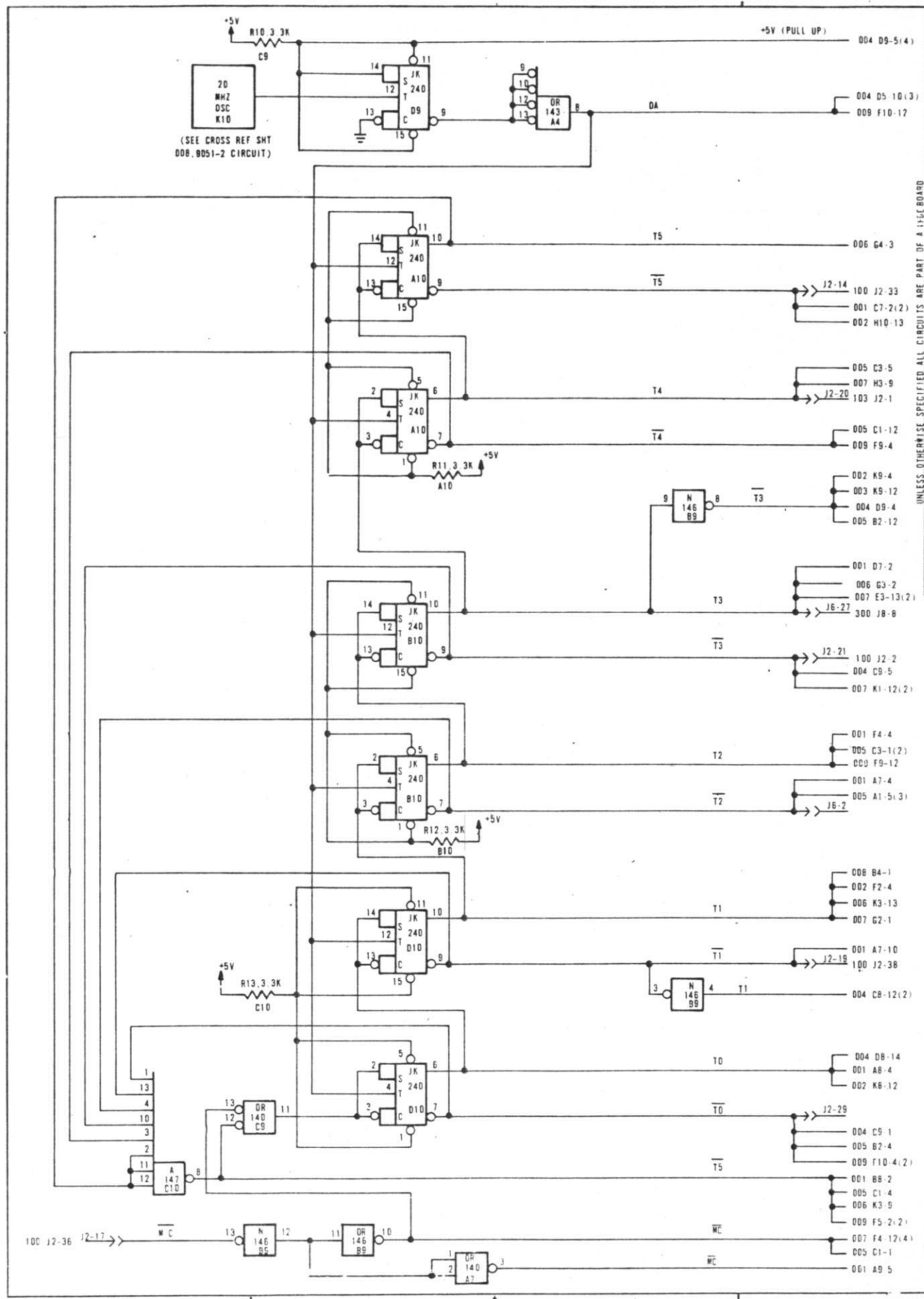
CODE IDENT		DWG NO	REV
15920		62164300	4
		CROSS REF NO	SHEET 26
		MEMORY TIMING, DISPLAY TIMING, & CONTROL	

BASIC CONTROL RING COUNTER DIAGRAM 000

20 MHZ OSCILLATOR — The 20 MHz oscillator is the master clock for the display station. It drives six timing-chain JK ff's via the JK ff D9. The sine-wave output of the oscillator has a 50 nsec time period. It drives D9 to produce a symmetrical square-wave output with a 100 nsec time period. This output, in turn, drives the timing chain to give the clock times T0, T1, T2, T3, T4, T5, and their complements. Each output pulse from the timing chain has a 100 nsec width with a 600 nsec time period. This time period is the time required to display one horizontal row of 5 dots plus a space of one dot for each character position in a scan line.



UNLESS OTHERWISE SPECIFIED ALL CIRCUITS ARE PART OF A 145 BOARD



BASIC CONTROL SCAN AND Y COUNTERS

DIAGRAM 001

SCAN COUNTER (C7) — The Scan Counter is an up binary counter which keeps track of which scan line is being scanned in a display line. See Section 4, Theory of Operation, for an illustration which shows the relationship between the scan lines and the count in the scan counter. It advances 12 times for each display line. At a count of 10_{10} (the bottom scan line in the display line), T3 sets the Advance Y ff, via gate B5-6, when the end of the scan line is reached (XTC). This ff uses its complementary outputs to put a logical 1 preset on the inputs to all of the stages of the Scan Counter and to supply a parallel load enable. At the next $\overline{T5}$, the Scan Counter loads logical 1's in all of its stages (count = 15_{10}). This is the top scan line in the display line. The outputs of the Scan Counter select 10-bit rows in the ROM character matrices. Also, they select one-half of this 10-bit word to form the video pulse train for each of two successive scan lines. Each half produces one horizontal 5-dot row in the character matrix of a display line.

ADVANCE Y FF (A6/A7) — For Y Counter counts 0 through 20_{10} , this ff allows the Y Counter to advance after the completion of 12 scan lines for each count. When the Y Counter = 21_{10} , the Advance Y ff allows the Y Counter to advance after the completion of only 10 scan lines. This makes a page or frame of 262 scan lines $(21 \times 12) + 10$. As mentioned in the Scan Counter paragraph, this ff provides a logical 1 preset and parallel load to enable to the Scan Counter following the completion of the last scan line of a display line.

Y COUNTER (D8/A9) — The Y Counter is an up binary counter which supplies the logic circuits with the vertical axis coordinate of the position of the CRT electron beam as it sweeps across the display screen. The logic circuits use this information to keep in step with the movement of the beam. It advances 22 times per page. Counts 0 through 15_{10} represent the 16 display lines. Counts 16 through 21 represent that time during which the CRT electron beam sweeps to the bottom of the screen, retraces to the top of the screen, and then sweeps down to the first display line. When the 10 scan lines which occur during Y Counter = 21_{10} are complete and the Advance Y ff is set, T0 gates through A8 to advance the Blink Counter.

BLINK COUNTER (K10) — The Blink Counter is an up binary counter which advances once per page. When the Blink Counter = 8_{10} , output pin 11 goes high to direct clear the Display Cursor ff which extinguishes the cursor display. This action gives a cursor blink rate of approximately three times per second.

ENABLE VERTICAL SYNC (C4) — Gate C4 provides the Enable Vertical Sync pulse for the CRT deflection circuits. The Y Counter and Scan Counter provide the inputs to gate C4.

BASIC CONTROL CURSOR X COUNTER

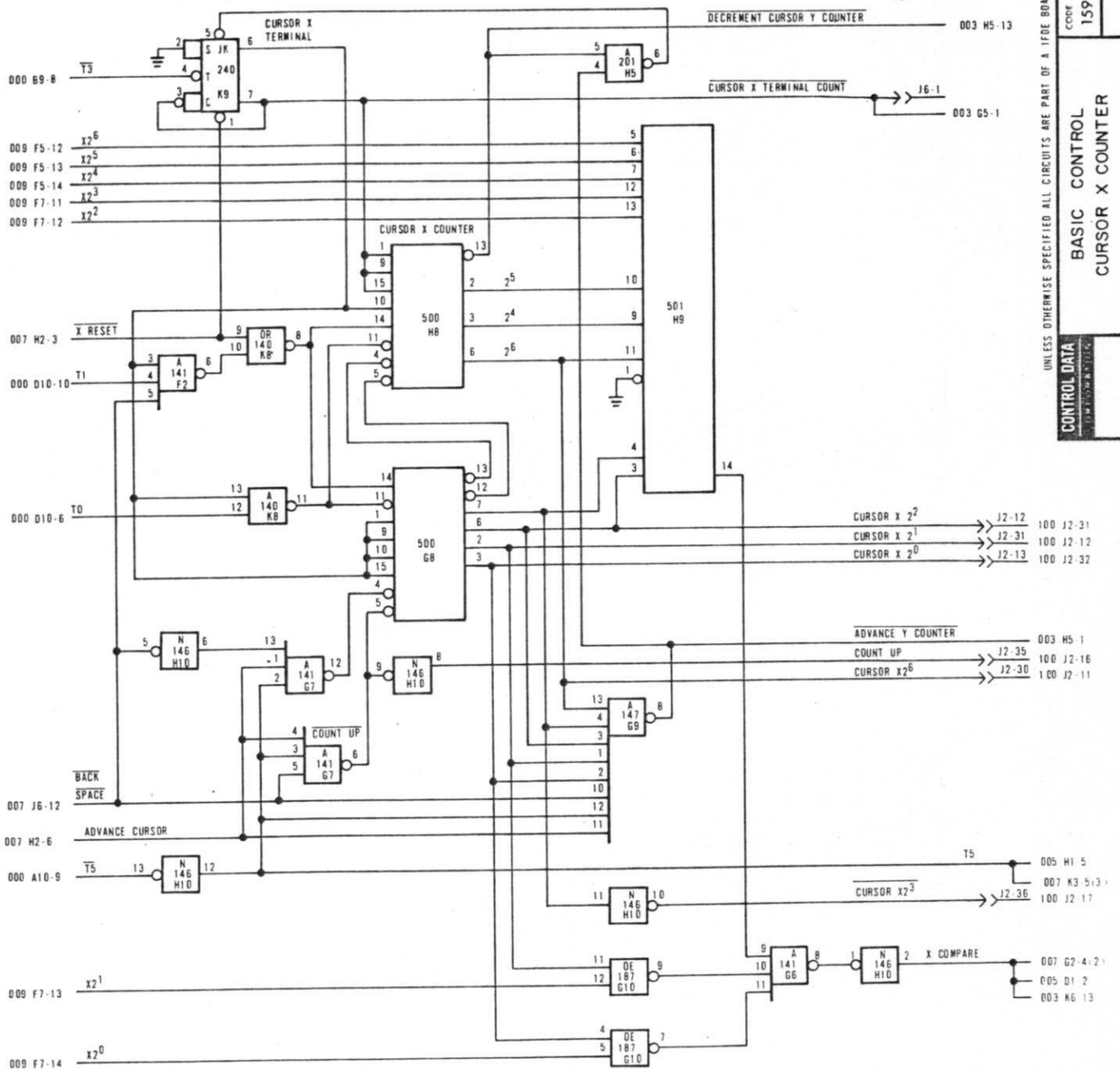
DIAGRAM 002

CURSOR X COUNTER (G8/H8) — The Cursor X Counter is an up/down binary counter which always contains the horizontal axis coordinate for the location of the cursor within the displayed data. It counts from 0 to 79_{10} to identify the 80 character locations in a display line at which the cursor may display. A count of 0 identifies the first character position in a display line. A count of 79_{10} identifies the last character position in a display line. When the count of the Cursor X Counter equals the count in the X Counter, an X Compare signal at H10 tells the display station circuits that the CRT electron beam and the logic circuit timing are at the horizontal axis coordinate of the cursor location. (However, before the cursor can display, a Y Compare must also occur (Diagram 003).) When the cursor moves one position to the right on the display screen, the Advance Cursor signal enables pin 4 of gate G7. As $\overline{T5}$ goes negative, G7 gates out a pulse on pin 6 to advance the Cursor X Counter by a count of one. The horizontal axis coordinate for the display of the cursor is now one position to the right of its previous location. If the cursor is in the last character position of the display line before it advances, the Cursor X Counter holds a count of 79_{10} . This count and the Advance Cursor signal enable gate G9. When $\overline{T5}$ goes negative, G9 outputs the Advance Y Counter signal on pin 8 to pin 4 of H5. This signal makes the Cursor Y Counter (Diagram 003) count up by one. This signal also passes through H5 to direct set the Cursor X Terminal ff K9. The pin 7 output of K9, Cursor X Terminal Count tells the circuits that the cursor has advanced beyond the last character position in a display line. This signal enables gate G6 at pin 3 (Diagram 003). The Cursor Y clock pulse input, (Diagram 003), to this gate makes the Cursor Y Counter (Diagram 003) count up by another count of one. In addition, setting C4 (Diagram 002) places an enable on pin 3 of F2 in this diagram. At T1, the Cursor X Counter resets to a count of zero. The cursor now displays in the first character position of the next lower line. At $\overline{T3}$, the Cursor X Terminal ff K9 clears to return to its initial condition. When the cursor moves one position to the left on the display screen (backspaces), the Advance Cursor signal enables pin 1 of gate G7. A Backspace signal on pin 13 provides the other enable. When $\overline{T5}$ goes negative, pin 12 of G7 outputs a pulse to make the Cursor X Counter count down by a count of one. The horizontal axis coordinate for the display of the cursor is now one position to the left of its previous location. If the cursor is in the first position of the display line when a backspace occurs, the Cursor X Counter counts down from a count of zero to a count of 256_{10} . This causes pin 13 of section H8 of the Cursor X Counter to go low. The output signal of pin 13, Decrement Cursor Y Counter makes the Cursor Y Counter count down by one. This also direct sets the Cursor X Terminal ff K9. This generates the signal Cursor X Terminal Count at pin 7 of K9. This signal permits the changing of the count in the Cursor Y Counter (Diagram 003). This time, the Cursor Y Counter counts down, at T1, by a count of one. Also, the pin 7 output of K9 supplies a count of 79_{10} preset to the Cursor X Counter. The output of pin 6 of K9 places an enable on pin 10 of the Cursor X Counter to allow a parallel load of the count of 79_{10} preset. It also enables pin 13 of gate K8 to allow $\overline{T0}$ to parallel load the count of 79_{10} into the Cursor X Counter. At $\overline{T3}$, the Cursor X Terminal ff clears to its initial condition. The cursor now displays in the last position of the preceding display line.

CURSOR X TERMINAL FF (K9) — As described by the preceding, at the end of the 80 character positions of a display line, the Cursor X Terminal ff sends the Cursor X Terminal Count signal to change the count in the Cursor Y Counter. It also supplies a count of 79_{10} preset to the Cursor X Counter for use as required.

X COMPARE — When the counts in the Cursor X Counter and the X Counter are equal, the X Compare circuitry connected to gate H9 recognizes this equality and sends the X Compare signal to the circuits of the logic module. This signal means that the logic circuit timing and the CRT electron beam have reached the horizontal axis coordinate for the location of the cursor.

UNLESS OTHERWISE SPECIFIED ALL CIRCUITS ARE PART OF A IFDE BOARD



BASIC CONTROL CURSOR Y COUNTER

DIAGRAM 003

CURSOR Y COUNTER (K7) — The Cursor Y Counter is an up/down binary counter which contains the vertical axis coordinate for the location of the cursor within the displayed data. It counts from 0 to 15_{10} to identify the eight display lines of 80 characters each. A count of 0 corresponds to the top display line on the screen (assuming no scroll has occurred). The even counts correspond to the other seven display lines with count 14_{10} identifying the bottom display line (assuming no scroll has occurred). The odd counts identify the display lines provided by the optional Expanded Memory Kit. This tells the logic module circuits that the CRT electron beam and the logic circuit timing are at the coordinate of the cursor location within the displayed data. When the cursor moves to the next upper display line, or from the top display line directly to the bottom display line, a pulse arrives at pin 4 of the counter to make it count down. With just the basic memory, two pulses occur to make it count down by a count of two. If the optional Expanded Memory Kit is included, only one pulse arrives to make it count down by a count of one. This is because the basic memory and the expanded memory display lines interlace on the display screen and in the logic circuit timing. When the cursor moves to the next lower display line (assuming it is not in the bottom display line before the move), two pulses arrive at pin 5 of K7 to make it count up by two (basic memory). Notice that the outputs of the Scroll Counter supply a preset to the stages of the Cursor Y Counter. Every time the cursor resets to the top display line, the Y Reset signal parallel loads the count in the Scroll Counter into the Cursor Y Counter. This makes certain that a Y Reset always results in the cursor displaying in the top display line of the displayed data. This must be done because a scroll causes an extra advance of the Y' Counter to place it one display line ahead in the timing scheme. Therefore, while the CRT electron beam is scanning the top display line on the screen, it could be displaying the data in any one of the lines in the memory. The memory line is displayed as the top line of data depending on how many scrolls have occurred.

CURSOR X TERMINAL — When only the basic memory is used, this signal allows an additional count by the Cursor Y Counter. This is in addition to the count supplied by the Advance Y Counter or Decrement Cursor Y Counter signals.

ADVANCE Y COUNTER — This signal makes the Cursor Y Counter count up by a count of one following the end of a display line.

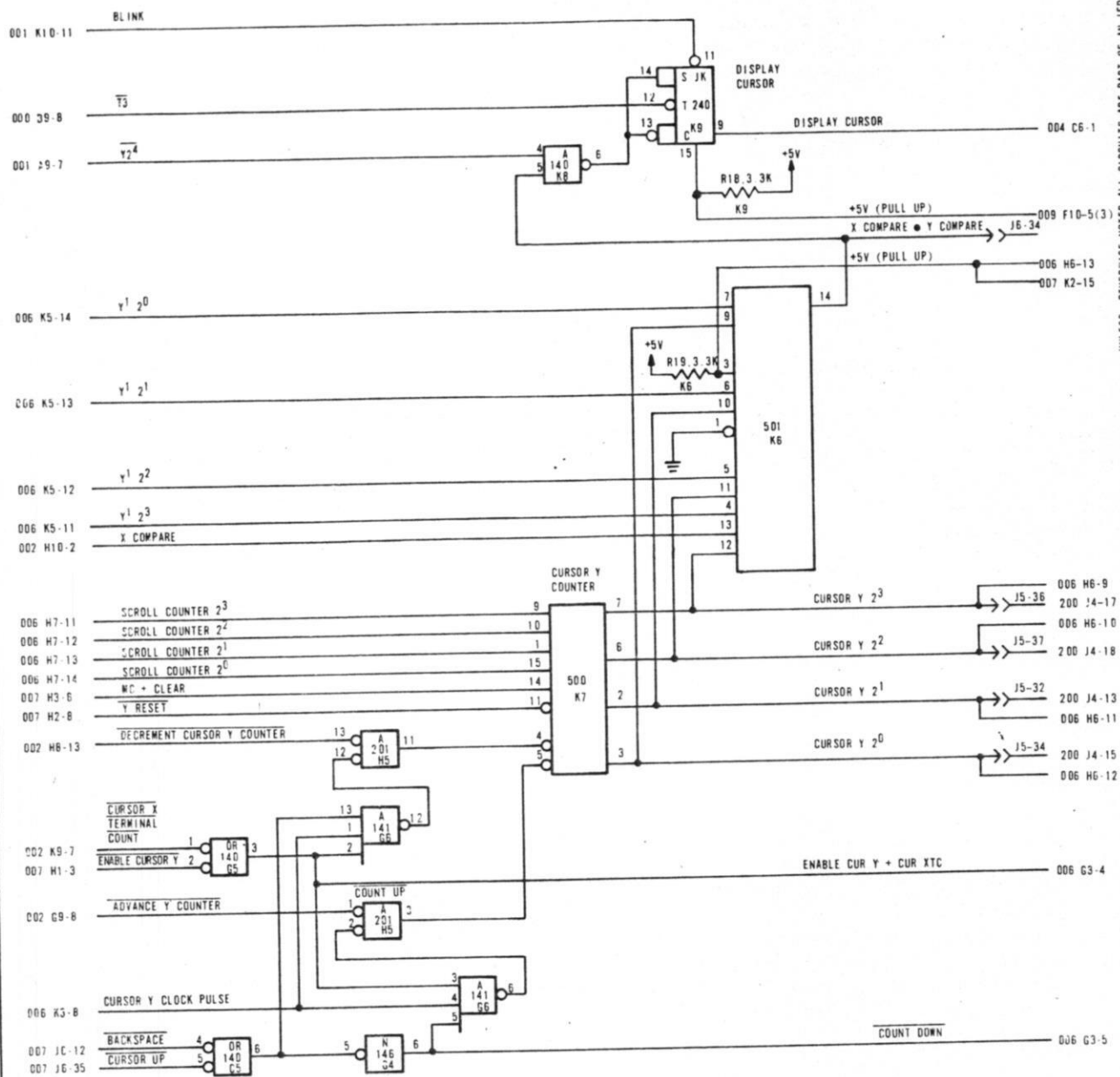
DECREMENT CURSOR Y COUNTER — This signal makes the Cursor Y Counter count down by a count of one if the cursor backspaces from the first position of a display line to the last position of the preceding display line.

ENABLE CURSOR Y — When an input control function Cursor Up, or Cursor Down occurs, this signal allows the Cursor Y Counter to count up or down as required.

CURSOR Y CLOCK PULSE — This line supplies a pulse every $\overline{T5}$ and T1 with the basic memory. If the Expanded Memory Kit is included, only $\overline{T5}$ appears. This is because with the expanded memory the cursor advances only one display line at a time. On the screen, the cursor moves from a display line provided by the basic memory to a display line provided by the expanded memory. With only the basic memory used, the cursor must step past the display line space used by the optional expanded memory.

DISPLAY CURSOR FF (K9) — When an X Compare and a Y Compare occur, the CRT electron beam is at the character location of the cursor within the displayed data. If the Y Counter (Diagram 001) has a count of less than 16_{10} , $\overline{T3}$ sets the Display Cursor ff to enable a gate (Diagram 004) which, in turn, gates if the CRT electron beam is scanning the correct scan line (Scan Counter = 9_{10}) to display the cursor. If so, the Display Cursor signal gates to make the video serializer shift out the pulse train to form the cursor on the display screen. The Display Cursor ff is direct cleared by the Blink signal to extinguish the display of the cursor. This occurs approximately three times per second.

X COMPARE • Y COMPARE — When the counts in the Cursor Y Counter and the Y' Counter are equal, the Y Compare circuitry connected to gate D1 recognizes this equality and sends the Y Compare signal to the circuits of the logic module. This signal means that the logic circuit timing and the CRT electron beam have reached the vertical axis coordinate for the location of the cursor.



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF AN ICD BOARD

CONTROL DATA

BASIC CURSOR	CONTROL Y COUNTER
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
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99	99
100	100

C

CODE IDENT

62164300 DWG NO

CROSS 003 SHEET 30

READ ONLY MEMORY AND VIDEO SERIALIZER

DIAGRAM 004

READ ONLY MEMORY (E6/E7) — The Read Only Memory (ROM) is a preprogrammed memory which provides the information bits which control the unblanking of the CRT electron beam. These ROM's contain a character matrix for each character in the repertoire of the logic module. The character matrices consist of 10-bit rows which supply a 10-bit word to the output lines of the ROM's. The primary ROM, E6, contains the matrices for codes 040₈ through 137₈. The secondary ROM, E9, contains the matrices for codes 140₈ through 177₈ and the three special character codes (033₈, 016₈, and 017₈).

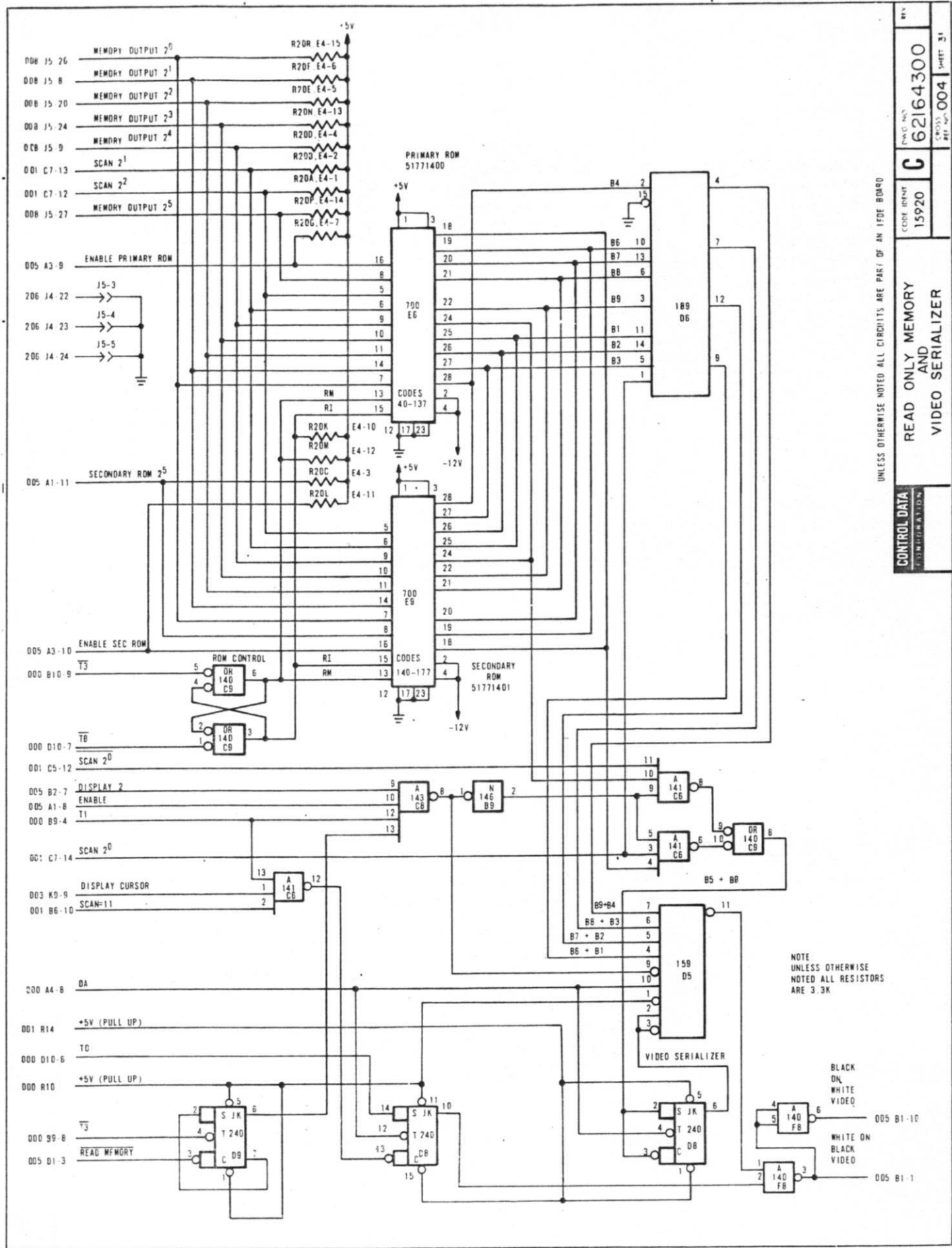
ROM CONTROL FF (C9/C9) — The ROM Control ff supplies the synchronous timing signals Read Input (RI, pin 3) and Read Memory (RM, pin 6) to the ROM's for use in sequencing their internal logic. Read Input allows the ROM to sample the read/write memory code for character matrix addressing. Read Memory allows the information bits in one of the 10-bit rows in a matrix to reach the output lines of the ROM.

ROM ENABLE — A circuit (Diagram 005) enables either the primary or the secondary ROM. If the read/write memory character code present on the ROM inputs has logical 1's or logical 0's in both bit positions 2⁵ and 2⁶, the secondary ROM enables. If the bits are complementary, the primary ROM enables.

VIDEO SERIALIZER (D5/D8) — The video serializer parallel loads 5 bits from the ROM's and shifts them out in serial form to unblank the electron beam of the CRT.

THE CIRCUIT IN ACTION — Because the electron beam displays only one horizontal 5-dot row of each character per scan line, a way is provided to select and use only five information bits, or one-half of the 10-bit word, at a time from the ROM's. To get five bits of information from the ROM's, the read/write memory places a character code on the character matrix address lines (Memory 2⁰ through Memory 2⁵) of the ROM's. As described by the preceding paragraph, ROM ENABLE, only one of the ROM's is enabled. While a character matrix address is available, the ROM Control ff (C9/C9) clears at T₀ to send a Read Input signal from pin 3 to pin 15 of the ROM. The ROM samples the character code on its input lines and selects a character matrix within the ROM. A 10-bit row is selected within the character matrix by the ROM inputs Scan 2¹ and Scan 2². These inputs change their combination input once for every two scan lines. Because of this, the 10-bit word which the ROM places on its output lines can supply the bits for two successive scan lines. Next, T₃ sets the ROM Control ff to send a Read Memory signal from pin 6 to pin 13 of the ROM. After a built-in delay, the 10-bit word from the row in the character matrix appears at the output lines of the ROM. The outputs of both ROM's are wired-OR and routed to gate D6. Also, the Scan Counter outputs Scan 2⁰ and is routed to D6. Scan 2⁰ is alternated logical 1 and 0. Therefore, it is possible to use Scan 2⁰ to select one-half of the 10-bit word and then the other half. Thus far, the circuit has succeeded in supplying five bits of information for use in unblanking the electron beam of the CRT to produce one horizontal row of 5 dots. To reach the CRT, the bits load into the video pulse-train output shift register (video serializer). This can happen only when the X Counter has a count of less than 80. This occurs during the display time of a scan line to send the Display 2 signal to pin 9 of gate C8. Pin 10 of C8 is high as a result of ROM enabling. Pin 13 is high if the logic module is not reading from the read/write memory to transmit character codes to an external equipment. The next T₁ gates through C8 on pin 8 to pin 9 of the video serializer, D5, to supply a parallel load enable for the information bits present as presets for the stages of the shift register. As ØA goes positive, the 4-bit shift register and the JK ff of the video serializer load the five information bits. Immediately, the first bit is present on pin 11 and pin 1 of F8. Pin 6 and pin 3 of F8 are complementary outputs. The next five clock pulses shift the remaining four bits to the output of A9. The last ØA clock pulse supplies a space between adjacent characters.

DISPLAY CURSOR (pin 12, C6) — When the Scan Counter = 9₁₀, and an X Compare and a Y Compare occurs, T₁ gates on pin 12 to cause the F8 to gate out the pulse train for the cursor. T₁ provides a set preset to pin 13 of D8. When ØA toggles D8, pin 10 of D8 stops output from the video serializer. This produces the bits for the cursor display.



BASIC CONTROL PROTECTED FIELD

DIAGRAM 005

INVERSE VIDEO CONTROL — The inverse video control circuits give a black-on-white data display on detection of a Start Inverse Video code (016_g). The black-on-white display clears on detection of an End Inverse Video code (017_g). This allows data highlighting within displayed messages. During the display time of a scan line (the count of the X Counter is less than 80₁₀), the Memory Control signal enables gate B7. When the character code at the outputs of the read/write memory is an End Field code, D4 gates to enable pin 2 of gate C3. T2 passes through this gate to set the Protected Field ff C2/C2. The output of pin 12 of this ff enables a gate to the set preset (pin 13) of the Holdover ff C1. It also enables a gate to the set preset (pin 3) of the White ff B2. T3 sets the White ff. The pin 9 output of this ff allows the Q3 video signal from the video serializer to gate to the CRT. This signal is inverted video. It produces the black-on-white display. When the White ff sets to gate the inverted video signal, it sends the Low Intensity signal to the emitter-base circuit of the Composite Video Driver circuit to decrease the forward bias of the NPN transistor. This reduces the amplitude of the video signal sent to the CRT for the black-on-white display. If an End Inverse Video code has not been detected before the end of the display time of a scan line, the black-on-white display continues for all 80 character positions. Then, the Display signal drops to furnish the White ff with a clear preset. T3 clears the White ff to end the black-on-white display. At the end of a scan line, the XTC signal permits T5 to clear the protected Field ff. The sequence repeats itself for the next scan line in the same display line. If an End Inverse Video code is not detected in the display line, the black-on-white field will continue when the electron beam of the CRT begins to scan the next lower display line. What causes this is the Advance Y signal arrives at T3 to supply a set preset to the Holdover ff. T4 sets this ff to hold the Inverse Video condition into the next display line. The XTC signal and T5 clear the Protected Field ff. However, T2 passes through gate C2 to set the Protected Field ff again. This, in turn, allows the White ff to set as soon as the electron beam reaches the first character position of the next display line. This is when the Memory Control signal raises to set the White ff to produce the inverted video signal. In the basic machine, the basic memory lines interlace with those of the optional Expanded Memory Kit. If the logic module does not include the expanded memory, it prevents the white field from displaying in an expanded memory line. This is the purpose of the Expanded Memory signal at pin 4 of D1. With only the basic memory, this line is a logical 1. Each time the Y Counter has an odd count (Y 2⁰ = logical 1), the White ff is direct set via gate D1. This blocks the white field from the expanded memory display line. If this black-on-white display were to continue through the last character position of the bottom display line, the Y2⁴ signal raises after the last scan line of the bottom display line to direct clear both the White and the Holdover ff's. The black-on-white display will not continue in the first character position of the top display line unless that character position contains a Start Inverse Video code. If an End Inverse Video character is detected before the end of the display time of a scan line, the code permits T4 to pass through gate C3 on pin 6 to clear the Protected Field ff. The output of pin 12 of this ff goes low which supplies a clear preset to the White ff. Next, T3 clears the White ff to end the black-on-white display. An End Inverse Video code also allows the Scan = 12_g signal to place a clear preset on pin 14 of the Holdover ff. If this were not done, the black-on-white display would end after the End Inverse Video code only to begin again in the next lower display line.

ROM ENABLE FF's (A3 and A3) — The ROM Enable ff's enable either the primary or the secondary ROM depending upon the logic state of the bit positions 2⁵ and 2⁶ of the read/write memory code. If they are both logical 1's or both logical 0's, the EXCLUSIVE OR gate G10 has a logical 0 output which supplies a set preset to the upper A3. T2 sets the ff to enable the secondary ROM. If Bits 2⁵ and 2⁶ are complementary, the output of the EXCLUSIVE OR gate is a logical 1 which supplies a clear preset to the upper ff A3. T2 clears the ff this time to enable the primary ROM. This circuit also furnishes an enable to the gating circuit for the parallel load signal for the video serializer (Diagram 004). This signal is called Enable. When the count of the Scan Counter is less than 8₁₀, pin 10 of gate A1 supplies the Enable signal. If the count of the Scan Counter is 8₁₀, then pin 6 of gate D4 furnishes the Enable Secondary ROM signal routes to this gate as it is the only ROM with character matrices that uses scan lines 7 and 8. If the Scan Counter = 9₁₀, the input of pin 1 blocks gate A4. This is done because scan line 9 is the cursor display line. If the Scan Counter = 10₁₀, the input of pin 1 blocks gate A4. This is done because no character formations use this line. The same is true when the Scan Counter = 15₁₀.

READ SEARCH FF (C1) — When the cursor changes position within the displayed data, the Read Search ff allows the character code above the new cursor position to load into the I/F output buffer (Diagram 101) during an X Compare. This ff sets to enable pin 1 of gate D1 and to gate the Busy signal (Diagram 006). When the X Compare occurs, an enable arrives on pin 2 of D1. This results in the gating of the signal Read Memory which permits the character code to load into the I/F output buffer.

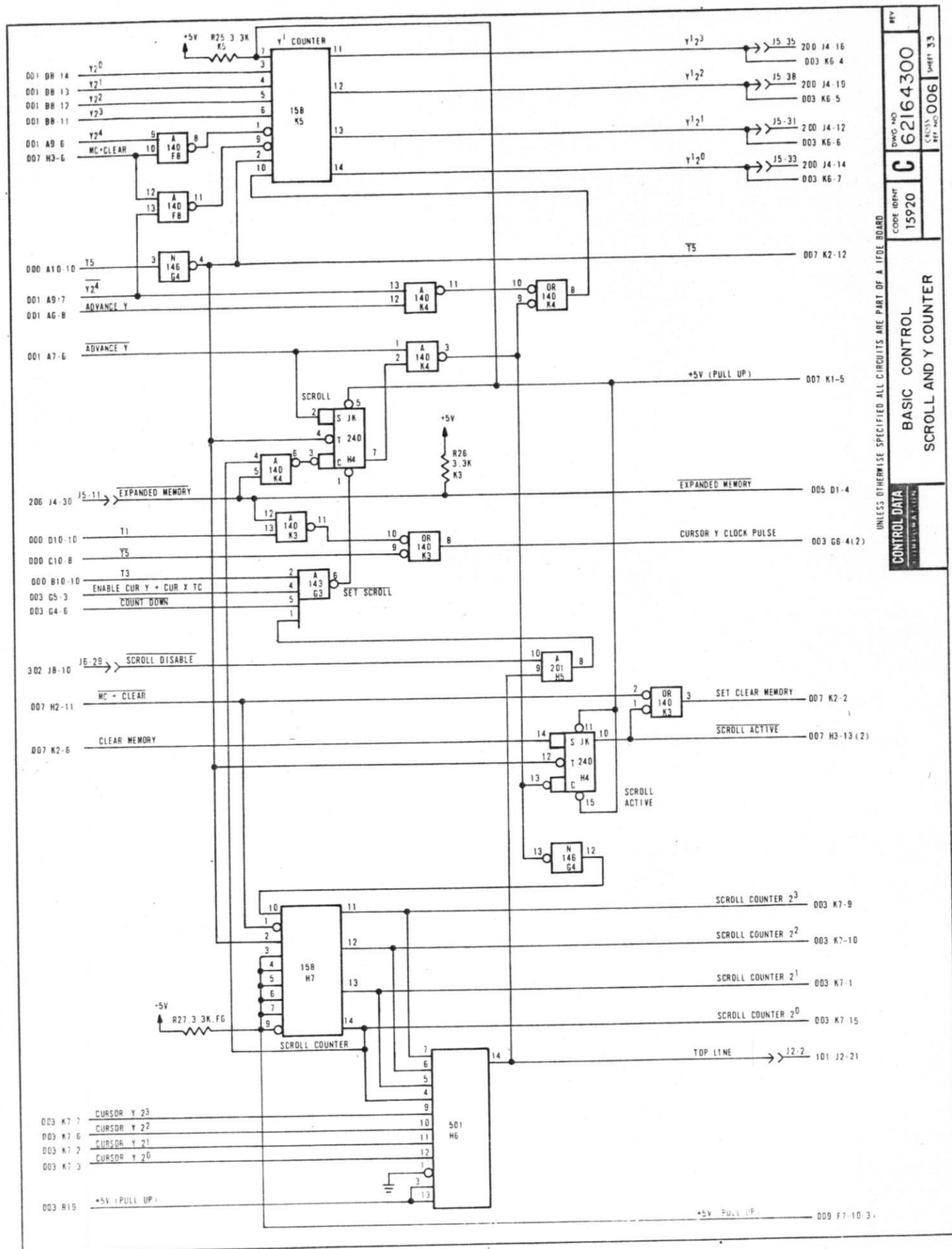
BASIC CONTROL SCROLL AND Y' COUNTER

DIAGRAM 006

Y' COUNTER (K5) — The Y' Counter is an up binary counter which selects the lines in the read/write memory to refresh and update the display on the screen of the CRT. It advances once for each display line. It counts from 0 to 15_{10} . When the count of the Y' Counter is even (0, 2, 4, 6, 8, 10, 12, or 14), it selects one of the eight memory lines of the basic memory (assuming no scroll has occurred). When the count is odd (1, 3, 5, 7, 9, 11, 13, or 15), it selects one of the eight memory lines of the optional Expanded Memory Kit (assuming no scroll has occurred). After the completion of the last scan line of a Display line, if the Y Counter has a count of less than 16_{10} , the Advance Y signal allows the Y' Counter to advance. The Cursor Y Clock Pulse output of gate K3 advances this counter at $\overline{T5}$. If the Expanded Memory Kit is not included, the Y' Counter still advances to provide an enable to the display line of the non-existent Expanded Memory. This is why the timing sends only the $\overline{T5}$ pulse to the Y' Counter and does not include the T1 pulse present at pin 13 of gate K3. If a scroll occurs, an enable which allows the counter to advance arrives via the input pin 9 of gate K4. $\overline{T5}$ will again advance the Y' Counter. Now, the counter is one display line in memory ahead of the position of the electron beam of the CRT. This causes all the data on the display screen to shift up one display line. Because the count of the Y' Counter is related to a scroll operation, the Y Compare circuit (Diagram 003) compares the output of this counter to that of the Cursor Y Counter to determine when the electron beam is at the vertical axis coordinate of the cursor location.

SCROLL COUNTER (H7) and SCROLL FF's (H4 and H4) — The Scroll Counter is an up binary counter which keeps track of the number of scrolls that have occurred. Then, when a Y Reset occurs to move the cursor to the top line of the displayed data, the count of the Cursor Y Counter is reset to the count held in the Scroll Counter. If the operator attempts to move the cursor from the bottom display line to a nonexistent next lower display line, a scroll happens. G3 gates at T3 to direct set the Scroll ff. This ff permits the extra advance of the Y' Counter to shift all the data up one display line. It allows the Scroll Counter to advance to keep track of the number of scrolls which have occurred and it supplies a set preset to pin 13 of ff H4. At $\overline{T5}$, the Scroll Active signal goes low to produce an X Reset (pin 13 of H3, Diagram 007) and to set the Clear Memory ff (Diagram 007) via pin 1 of gate K3 in this diagram. The Scroll Active signal also gives a Busy signal (pin 13 of G3, Diagram 007). The result of a Scroll is to move all the data up one display line, to clear the bottom display line (this memory line fills with Space codes), and to reset the cursor to the first character position of the bottom display line.

CLOCK PULSE CIRCUIT (K3 and K3) — This circuit supplies the pulse T5 to advance the Y' Counter and the Scroll Counter. It also supplies T5 to change the count in the Cursor Y Counter. If the optional Expanded Memory Kit is not a part of the display station, it also sends T1 to change the count of the Cursor Y Counter. This is because the display lines of the basic memory and the expanded memory interlace on the display screen. With only the basic memory, two pulses are required to change the count of the Cursor Y Counter to move the cursor from one basic memory display line to another.



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CONTROL DATA
INTELLIGENCE

BASIC CONTROL
SCROLL AND Y COUNTER

CODE IDENT
15920

DWG NO
C 62164300

REV
CROSS
REF NO
006

SHEET 33

BASIC CONTROL CURSOR MOVEMENT

DIAGRAM 007

INCREMENT CURSOR FF (pin 10, K1) — The logic module uses this ff as the control point for controlling those operations which result in the movement of the cursor. It sets during a Cursor Up, Cursor Down, Reset, Skip, or Backspace input control function. It gates out the Advance Cursor signal to change the count of the Cursor Y Counter.

END OF OPERATION FF (pin 6, K1) — This ff directs the clearing of the interface input buffer (Assembly Register) at the completion of an input control function. The output of pin 7 of this ff then enables the setting of the Read Search ff (Diagram 005) to load the next character code into the Disassembly Register (Diagram 102).

WRITE SEARCH FF (pin 10, K2) — During either an input data function or a clear memory operation, this ff sets to allow the next X Compare to gate the Write signal to the read/write memory to enter a code. It also gates the Advance Cursor signal to advance the cursor one character position.

MASTER CLEAR OR CLEAR FF (pin 6, H2/H3) — A local master clear or a Clear signal sent from an external equipment sets this ff. It then returns all the circuits to their initial condition. It also results in the setting of the Clear Memory ff to permit the filling of all the lines of the read/write memory with Space codes.

CLEAR MEMORY FF (pin 6, K2) — This ff sets to fill either one line or all of the lines of the read/write memory with Space codes. It is this ff which forces the Space codes at the inputs to the memory lines. It fills only one line in memory with Space codes if the Master Clear ff is not set. When the X = 150 signal (X Counter = 10410) raises, T5 clears the Clear Memory ff.

BUSY SIGNAL (pin 8, G3) — A write, read, scroll, or clear memory operation generates a Busy signal to prevent the station from accepting another function until the present one is complete.

X RESET SIGNAL (pin 3, H2) — The X Reset signal resets the Cursor X Counter to zero and clears the Cursor X Terminal ff (Diagram 002). It also permits setting the Read Search ff (Diagram 005) to allow the next X Compare to gate the Read Memory signal. Then, the character above the new cursor location loads into the Disassembly Register (Diagram 102).

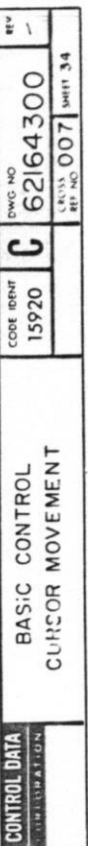
Y RESET SIGNAL (pin 8, H2) — This signal sets the count of the Cursor Y Counter equal to the count of the Scroll Counter. This makes certain that the Y Reset places the cursor in the top display line on the display screen in case a scroll has occurred at some time previously.

ADVANCE CURSOR SIGNAL (pin 6, H2) — This signal allows the changing of the count in the Cursor X Counter (Diagram 002). It also permits the setting of the Read Search ff (Diagram 005) to load the character code above the new cursor position into the Disassembly Register (Diagram 102).

WRITE SIGNAL (pin 3, E3) — This signal directs the Write Line Select 1-of-8 decoder in the read/write memory to select a memory line. At the next X Compare, a code will enter the memory at the present cursor location in the displayed data.

ENABLE CURSOR Y SIGNAL (pin 3, H1) — This signal allows the count in the Cursor Y Counter (Diagram 003) to change to move the cursor from one display line to another.

INPUT CONTROL FUNCTIONS — After detection in the interface, the input control functions, Cursor Up, Cursor Down, Reset, Skip, Backspace, Line Clear, and Clear enter this circuit to start the circuit action required by their specific functions.

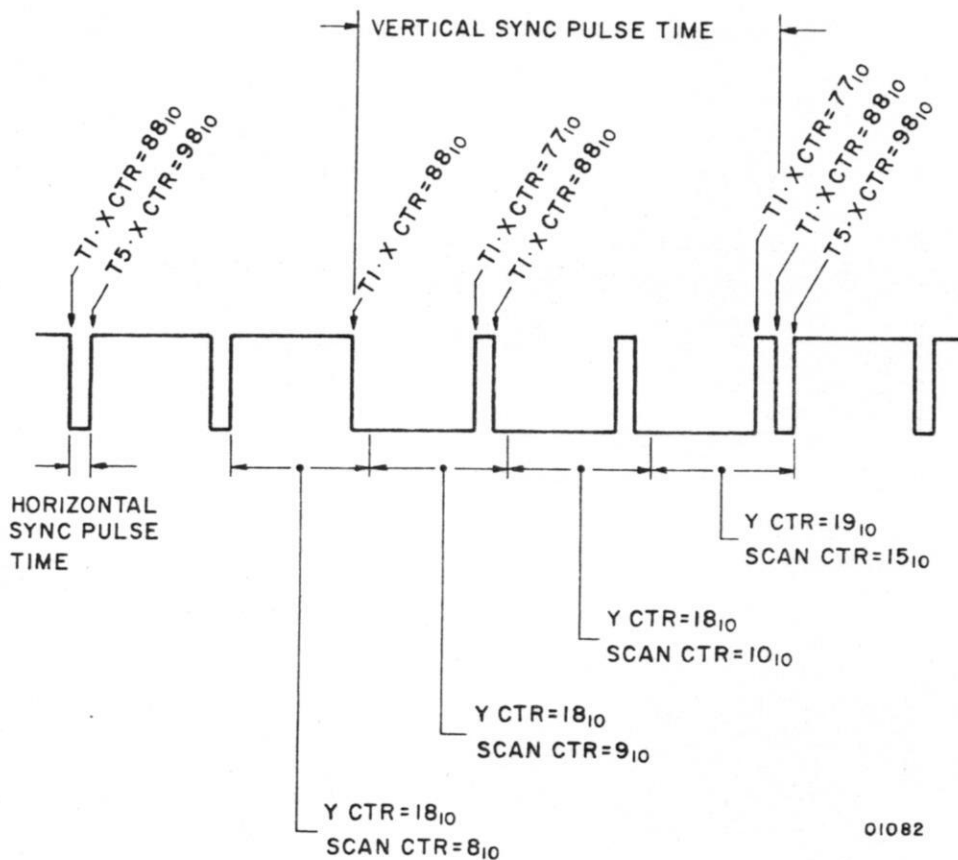


BASIC CONTROL DATA PATHS, BASIC CONTROL CURSOR MOVEMENT
DIAGRAM 008

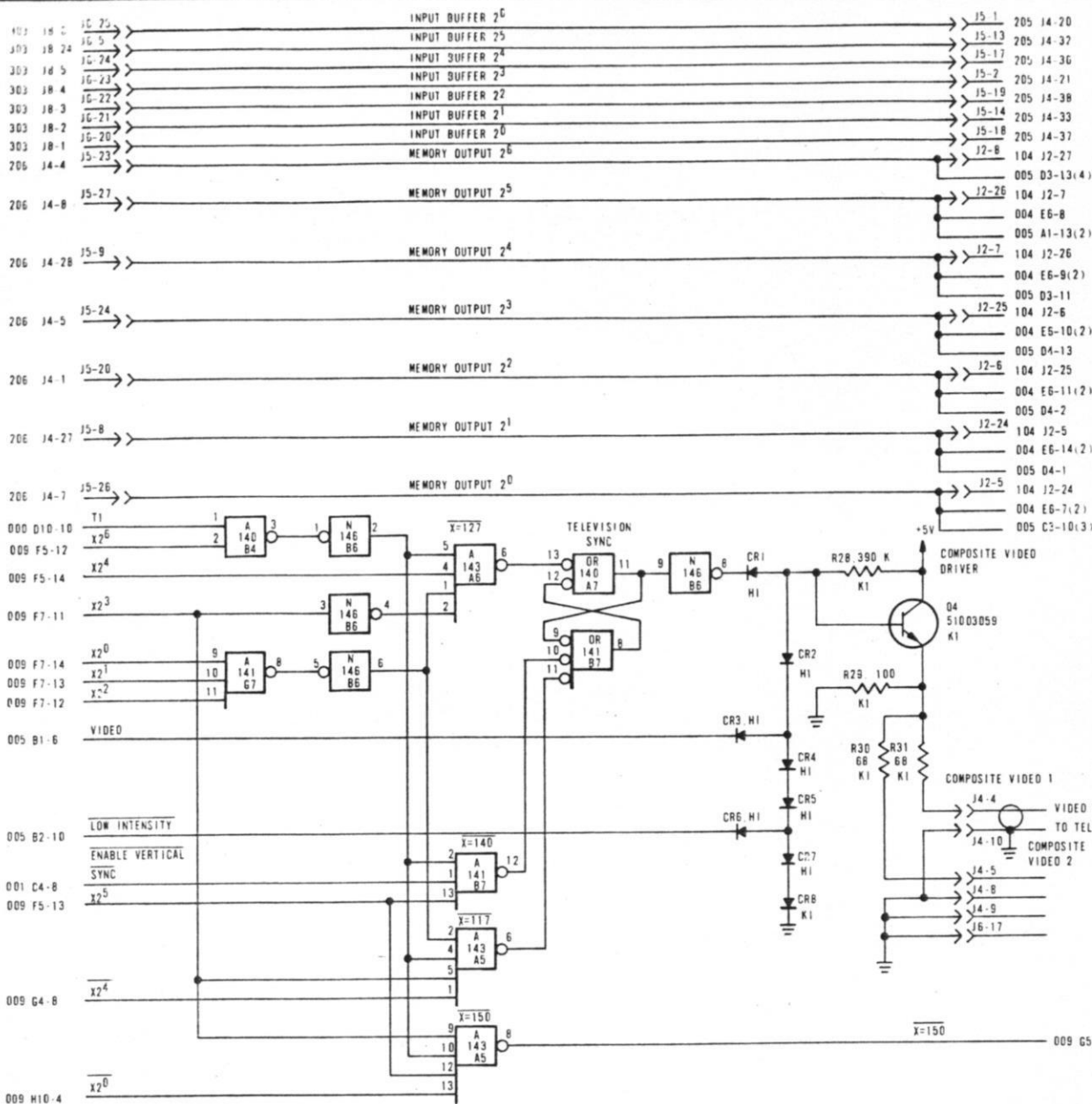
INPUT BUFFER $2^0 - 2^6$ SIGNALS — These seven signal lines carry data from the Assembly Register (Diagram 303) to the Display Memory input (Diagram 205).

MEMORY OUTPUT $2^0 - 2^6$ SIGNALS — These seven signal lines carry data from the Display Memory output multiplexers (Diagram 206) to interface Data Control Gates (Diagram 104) and data control circuits (Diagrams 004 and 005).

TELEVISION SYNC FF (A7/A8) — X Counter, and Enable vertical inputs to the Television Sync ff generate the horizontal and vertical sync pulses to synchronize the deflection circuits of the CRT to the logic circuit timing. The sync pulses are shown below. The waveform shown appears at the base and the emitter of transistor Q4.



COMPOSITE VIDEO DRIVER CIRCUIT (K1Q4) — The circuit of transistor Q4 combines the sync pulse output of the Television Sync ff with the output of the video serializer. The output of this emitter-follower circuit passes through a coaxial cable to the deflection circuits of the CRT. During a black-on-white display, the Low Intensity signal to the base of the transistor goes low to reduce the emitter-base forward bias. This reduces the amplitude of the video signal.



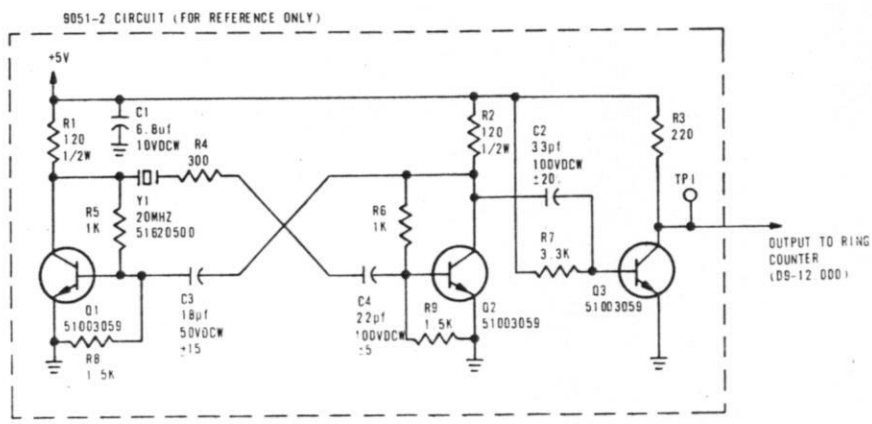
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF AN IDE 90ARD

CONTROL DATA CORPORATION

BASIC CONTROL DATA PATHS,
BASIC CONTROL
CURSOR MOVEMENT

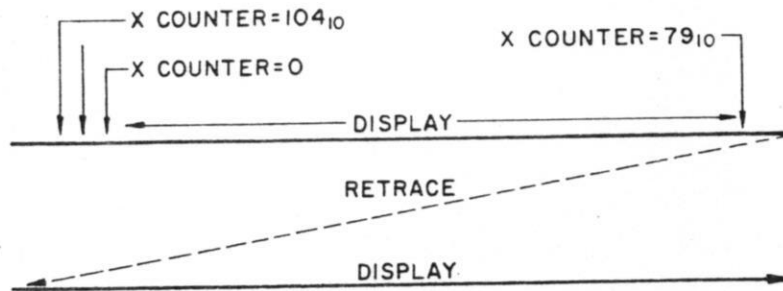
REV
C
15920
CROSS
REF NO
008
SHEET
35

NOTE
UNLESS OTHERWISE NOTED
ALL DIODES ARE 51001239



BASIC CONTROL X COUNTER DIAGRAM 009

X COUNTER (F5/F7) — The X Counter is an up binary counter which supplies the logic circuits with the horizontal axis coordinate of the position of the CRT electron beam as it sweeps across the display screen. The logic circuits use this information to keep in step with the movement of the electron beam. It advances 106 times per scan line. Counts 0 through 79₁₀ represent the 80 character positions in a display line. Counts 80₁₀ through 98₁₀ represent the normal horizontal sync pulse time. At advance 105, all stages fill with logical 1's. At advance 106, the counter returns to a count of zero and outputs the X Terminal Count (XTC) signal to identify the end of one complete scan line.

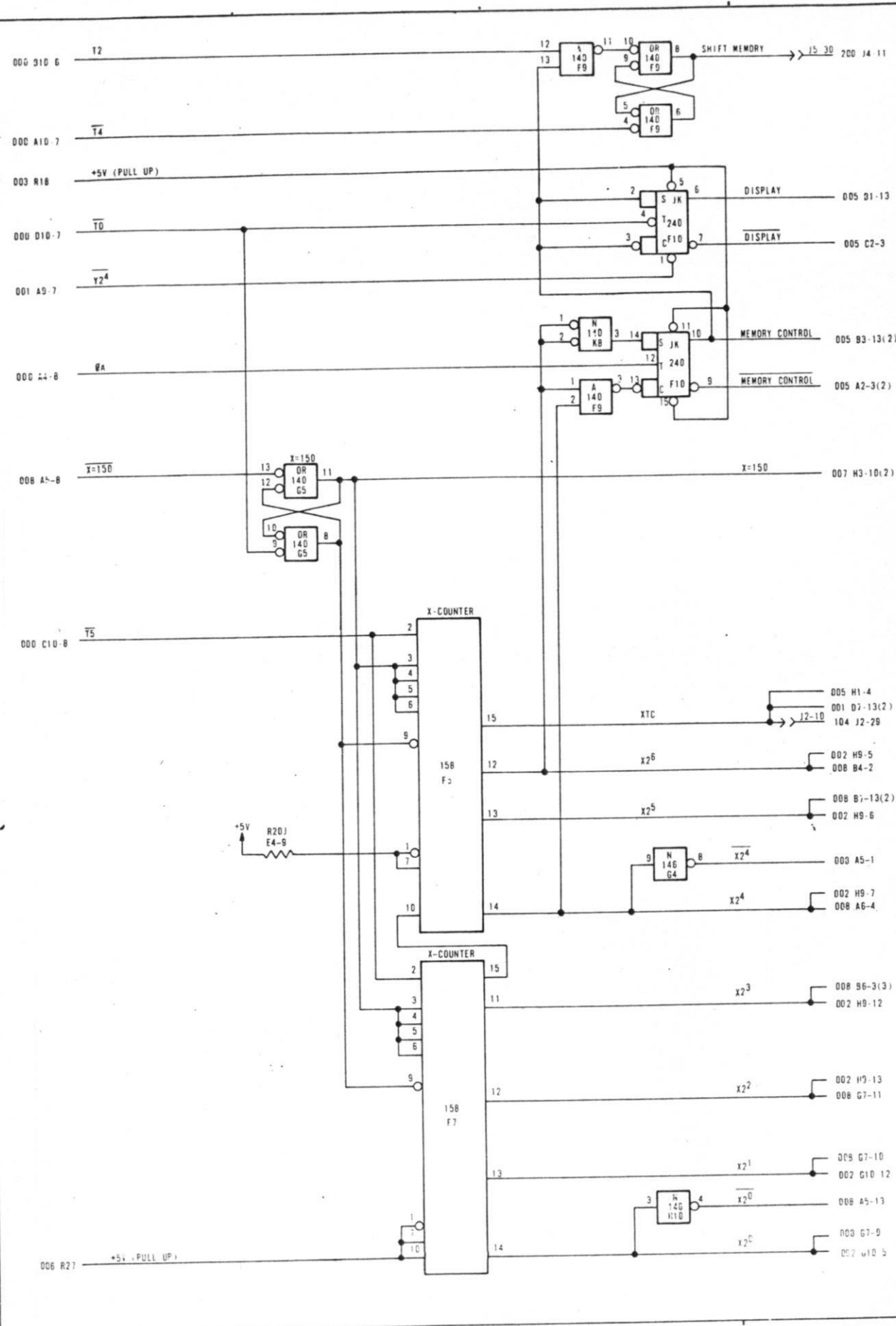


X = 150g (G5/G5) — When the X Counter = 104₁₀, this ff sets to furnish a logical 1 preset to all the stages of the X Counter. The logical 0 output supplies a parallel load enable to the X Counter. At the next T5, the X Counter parallel loads logical 1's in all of its stages. This makes it possible for the next T5 to produce an XTC signal on pin 15 to signal the other circuits of the end of one complete scan line.

MEMORY CONTROL FF (F10) — During the display time of a scan line, this ff permits the shifting of the bits stored in the shift registers of the read/write memory by enabling the Shift Memory ff. Clock pulse 0A sets it at X Counter = 0 (beginning of display time of scan line). It clears it at X Counter = 80₁₀ (end of display time of scan line). This ff controls the Display ff.

DISPLAY FF (F10) — During the display time of a scan line, this ff allows the gating of information bits from the ROM to the inputs of the video serializer. If a black-on-white field is being displayed, it clears the White ff at the end of the display time. This ends the black-on-white display after the last character position.

SHIFT MEMORY FF (F9/F9) — During the display time of a scan line, it provides the clock pulses to recirculate (shift) the bits in the shift registers of the read/write memory.



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REV	62164300
DWG NO	62164300
CODE IDENT	C
15920	
UNIT NO	009
SHEET	35

BASIC CONTROL, X COUNTER

CONTROL DATA CORPORATION

CONN NO	SIGNAL	CONN NO	SIGNAL	CONN NO	SIGNAL	CONN NO	SIGNAL
J2-1	CLEAR "CLEAR MEMORY"	J3-1	+5V	J5-1	INPUT BUFFER 25	J6-1	CURSOR X TERMINAL COUNT
J2-2	TOP LINE	J3-2		J5-2	INPUT BUFFER 23	J6-2	T2
J2-3		J3-3	+12V	J5-3	GROUND	J6-3	READ MEMORY
J2-4		J3-4	-12V	J5-4	GROUND	J6-4	
J2-5	MEMORY OUTPUT 20	J3-5	GROUND	J5-5	GROUND	J6-5	INPUT BUFFER 25
J2-6	MEMORY OUTPUT 22	J3-6	(KEYED PIN)	J5-6	MEMORY MULTIPLEX 23	J6-6	LINE CLEAR
J2-7	MEMORY OUTPUT 24	J3-7		J5-7	MEMORY MULTIPLEX 21	J6-7	INPUT
J2-8	MEMORY OUTPUT 26	J3-8	+12V	J5-8	MEMORY OUTPUT 21	J6-8	Y20 EXPANDED MEMORY
J2-9		J3-9	-12V	J5-9	MEMORY OUTPUT 24	J6-9	FUNCTION CHAR
J2-10	ATC	J3-10	GROUND	J5-10	MEMORY MULTIPLEX 24	J6-10	
J2-11				J5-11	EXPANDED MEMORY	J6-11	
J2-12	CURSOR X 22			J5-12	MC + CLEAR	J6-12	BACKSPACE
J2-13	CURSOR X 20			J5-13	INPUT BUFFER 25	J6-13	RESET
J2-14	T5			J5-14	INPUT BUFFER 21	J6-14	SKIP
J2-15				J5-15	READ MEMORY	J6-15	BUSY
J2-16				J5-16	CLEAR MEMORY	J6-16	
J2-17	MC			J5-17	INPUT BUFFER 24	J6-17	GROUND
J2-18				J5-18	INPUT BUFFER 20	J6-18	CLEAR
J2-19	T1			J5-19	INPUT BUFFER 22	J6-19	CLEAR INPUT BUFFER
J2-20	T4			J5-20	MEMORY OUTPUT 22	J6-20	INPUT BUFFER 20
J2-21	T3	J4-1	(KEYED PIN)	J5-21	MEMORY MULTIPLEX 22	J6-21	INPUT BUFFER 21
J2-22		J4-2		J5-22	MEMORY MULTIPLEX 26	J6-22	INPUT BUFFER 22
J2-23		J4-3		J5-23	MEMORY OUTPUT 26	J6-23	INPUT BUFFER 23
J2-24	MEMORY OUTPUT 21	J4-4	COMPOSITE VIDEO 1	J5-24	MEMORY OUTPUT 23	J6-24	INPUT BUFFER 24
J2-25	MEMORY OUTPUT 23	J4-5	COMPOSITE VIDEO 2	J5-25	MEMORY MULTIPLEX 20	J6-25	INPUT BUFFER 26
J2-26	MEMORY OUTPUT 25	J4-6		J5-26	MEMORY OUTPUT 20	J6-26	
J2-27		J4-7	50 HZ	J5-27	MEMORY OUTPUT 25	J6-27	T3
J2-28		J4-8	GROUND	J5-28	MEMORY MULTIPLEX 25	J6-28	
J2-29	T6	J4-9	GROUND	J5-29	WRITE	J6-29	DISABLE SCROLL
J2-30	CURSOR X 26	J4-10	GROUND	J5-30	SHIFT MEMORY	J6-30	
J2-31	CURSOR X 21			J5-31	Y1 21	J6-31	SET READ SEARCH
J2-32				J5-32	CURSOR Y 21	J6-32	CONTROL KEY
J2-33	X RESET			J5-33	Y1 20	J6-33	X COMPARE • Y COMPARE
J2-34	COUNT UP			J5-34	CURSOR Y 20	J6-34	CURSOR UP
J2-35	CURSOR X 23			J5-35	Y1 23	J6-35	CURSOR DOWN
J2-36	BLINK T C			J5-36	CURSOR Y 23	J6-36	
J2-37				J5-37	CURSOR Y 22	J6-37	
J2-38				J5-38	Y1 22	J6-38	

DATA SET DRIVERS AND RECEIVERS

DIAGRAM 100

RECEIVE DATA (Pin 1, D2) — Data from remote equipment arrives serially on the Receive Data line. This interface operates in accordance with EIA Standard RS 232-C. This means that when no data is arriving, the necessary interfacing modem holds the Receive Data line more negative than -3 volts to produce a logical "1" condition (marking). In this condition, pin 3 of Receiver D2 passes an internal logical "1" (approximately +5 volts). When a data word arrives, the serial bits of the data word must be preceded by a start bit. The start bit is the condition on the Receive Data line when it changes from marking to a logical "0" (spacing) condition for one bit time (eg, 3.33 millisec at baud interface rate, see Diagram 300). The start bit alerts the logic module to the following data word bits.

DATA SET READY (Pin 10, D2) — This is an RS 232-C modem interface control signal. With pin 10 at a logical "1" condition (more negative than -3 volts, OFF), the communications modem associated with the logic module is not in operating condition for communications between remote equipment and the module. This condition causes an internal logical "1" on pin 8, D2 which prevents illumination of the receive active indicator and prevents Receive Data bits from changing logic states at the output of gate D10. Thus a start bit will not pass D10 when the associated data set is not ready. With pin 10, D2 at a logical "0" condition (more positive than +3 volts, ON) the Receive Active indicator illuminates and an enable is applied to gate D10 to allow receive data start bit and following bits.

RECEIVE DATA CIRCUIT IN ACTION — When the data set is ready, a start bit arriving on the Receive Data line will pass through gate D2 pin 11 as a logical "1" (logic high, approximately +5 volts). This applies a preset to Loop Enable ff, B1 pin 14 (Diagram 102). At the end of the next scan line (XTC) and T5, the Loop Enable ff sets applying an enable to pin 13, C1 back on Diagram 100. Now, received data will pass to the Assembly Register (Diagram 303), and to printer data channel driver A9 (Diagram 302). Received data also goes to the Receive Clock (Diagram 301).

REQUEST TO SEND (pin 3, D10) — This is an RS 232-C modem interface control signal. With pin 3 at a logical "0" condition (more positive than +3 volts, ON) the logic module is asking to send data to an associated modem. A Clear to Send active signal from the modem must arrive at the logic module in response to the Request to Send before the logic module may actually send data via the Send Data line. A Request to Send signal occurs only when the logic module is not operating in Local mode (gate B2, pin 6, Diagram 102) and when no Block Transfer for output to printer channel is in process (A1/A1, Diagram 103).

CLEAR TO SEND (pin 4, D2) — This is an RS 232-C modem interface control signal. With pin 4 at a logical "0" condition (more positive than +3 volts, ON) the communications modem is ready to receive information from the logic module. This signal becomes logical "0" in response to the Request to Send signal within 8 to 210 milliseconds after the Request to Send signal is made positive. Time variation is due to turnaround time of the modem common carrier. The Clear to Send remains positive until the Request to Send line is made negative on the modem interface. When Clear to Send is active, the Send Active indicator illuminates and Clear to Send applies an enable on pin 11, A3 (Diagram 102) to allow keyboard data strobes thus clearing the way for sending keyboard data inputs to remote equipment.

SEND DATA (pin 6, D10) — The logic module transmits data words to the RS 232-C modem via the Send Data line. When no transmission is in process, the logic module holds pin 6 in a logical "1" condition (more negative than -3 volts, marking). When Break is not active (pin 5, D10), serial data bits for transmission, beginning with a start bit (pin 6 made more positive than +3 volts), are supplied to the Send Data line from the Disassembly Register output gate A3, pin 6 (Diagram 102).

ALARM CIRCUIT — Cursor X Counter = 71₁₀ places an enable on gate A10. The next cursor advance allows T5 to pass through the gate via the Count Up signal. Output of A10 direct sets the B8 ff at pin 11. This ff's output pin 10 places a set preset on pin 2 of the second B8 ff. The next positive Blink T.C. signal (occurs approximately 4 times per second at T0) sets the second ff. Output of this second ff on pin 6 enables an audio tone generator to signal an operator that eight character positions remain from the present cursor position to the end of the display line. Ring Bell function from Function Decoder A3 (Diagram 302) will also preset ff B8 on pin 11. The rest of the circuit operation is the same as described above for Cursor X Counter = 71₁₀ except this action alerts an operator as a result of the Ring Bell function code being received from remote equipment. This may be used for operator alert of incoming messages.

PRINTER BLOCK TRANSFER CONTROL

DIAGRAM 101

PRINTER BLOCK TRANSFER CONTROL — Block transfer ff's B5 and B5 and associated gates control the block transfer of data stored in the refresh memory (Diagrams 200 through 206) to the printer channel (top portion of Diagram 302). When Start Bit is not present, Disassembly Register is not active, printer line is not active, and Print Key signal is present signifying a request for a printout of all data stored in refresh memory, then gate D3, pin 8 applies a preset to primary Block Transfer ff B5, pin 13. The end of Xmit Sync (occurs at T1) toggles this ff at pin 12. Block transfer operation now begins with primary Block Transfer ff pin 9 outputting Block Transfer signal and pin 10 outputting Block Transfer signal. If the logic module is not presently active with the printer channel (Terminal Active line logic high), gate B4, pin 8 outputs Block Transfer Reset signal which enables the Reset Cursor function and the Input operation (Diagram 302, gate C6, pin 6 and gate C3, pin 3). Block Transfer from ff B5, pin 10 passes through gate C5, pin 11 to disable scroll operation so Reset Cursor will be at first character position of top display line. Scroll operation is also disabled so, at end of print when the cursor passes the last character in the bottom display line to reset to the first character of the top line and stop, a scroll will not occur.

With block transfer operation in process, when the data transfer is past top display line data, gate B4 pin 6 applies a preset to ff B5 pin 3. The end of the next TT triggers this ff so its pin 7 output becomes logical high. This ff cannot change state during block transfer operation. It is used to clear the primary Block Transfer ff at the end of a block print operation when the cursor returns to top line. When Top Line occurs, the following T5 causes gate A4 pin 6 to pass a force clear signal which clears the Block Transfer ff at pin 11. Pin 10 output of primary Block Transfer ff now applies a preset on pin 2 of ff B5. The end of the following TT toggles ff B5 pin 7 to remove the force clear from primary Block Transfer ff pin 11.

PARALLEL ENABLE (pin 4, C7) — During the time Block Transfer ff is set, gate C3 pin 3 is allowed to pass the Read Memory signal (originating from gate D1 pin 3, Diagram 005) such that it becomes the Parallel Enable for the Disassembly Register (B6/B7 Diagram 102). Thus, character codes stored in memory are made available to the serial printer interface via the Disassembly Register and serial data gate A1 pin 11 (Diagram 102).

ENABLE START BIT FF (C6) — While the Block Transfer ff is set, each character's Read Memory signal will pass gate A4 Pin 12 at T3 to force set Enable Start Bit control ff C6 at pin 5. Read Memory signal also passes through gate A5 to pin 6 to provide Shift Disassembly Register signal. If the Disassembly Register is not active with the previous character code and the printer is not busy, gate C3 pin 11 passes the signal Enable Start Bit to apply a preset to Start Bit ff B3 pin 2 (Diagram 102). At the end of Xmit Sync, Start Bit ff B3 sets (Diagram 102) and Enable Start Bit control ff C6 receives a clear preset on pin 3. At the end of Transmit Clock signal Transmit Lockout, start bit control ff clears. With Block Transfer ff set, and Enable Start Bit Control ff clear, Start Bit signal passes through gate C9 pin 6 to provide Shift Disassembly Register signal.

SCROLL DISABLE (pin 11, C5) — A switch located off the interface board enables Scroll Disable to prevent display lines from scrolling up one line in display memory each time cursor moves from last character position to bottom display line.

LOOP ENABLE FF (B1) — The Loop Enable ff determines whether the Assembly Register (B2/B3, Diagram 303) loads with remote data only (data incoming from modem interface) or if it loads with data from the Disassembly Register. In Half Duplex, Local, or Print Block Transfer operating modes, the Assembly Register loads from the Disassembly Register. This allows keyboard input displayable data codes to be written directly into refresh memory and also enables keyboard input function codes to be acted upon by the basic control circuits. In addition, all codes read from memory for Print Block Transfer are rewritten in refresh memory. In Half Duplex, Local, or Print Block Transfer is the operating mode, gate B2 pin 8 provides an enable to gate B2 pin 13. If the Assembly Register has been cleared at the end of the last code input, no start bit is present, and the Disassembly Register is not active, then Half Duplex, Local, or Print Block Transfer will not apply a preset to pin 13 of Loop Enable ff B1. The XTC output at time T5 from the X-Counter F5/F7 (Diagram 009) provides a high trigger to pin 12 of ff B1. This toggles Loop Enable ff output pin 9 to logic high and this signal supplies an enable to gate A1, pin 12. In this condition, all serial data from the Disassembly Register will pass through gate A1 pin 11 and then to gate C1 pin 1 (Diagram 100). At this point the data is handled by the Assembly Register the same as if it were incoming Receive Data. With the Loop Enable ff set in this manner (for Half Duplex, or Print Block Transfer operation), if a logical "1" Start Bit should arrive on the Receive Data line to place a preset on Loop Enable ff pin 14, the following will occur: 1) D7 (Diagram 301) is triggered and the resulting Clear Active 2 signal force clears Block Transfer ff (Diagram 101). This stops a print block transfer operation if it is in process. 2) When XTC drops, Loop Enable ff sets to provide Loop Enable signal from pin 10 to Receive Data gate C1 pin 13. This allows Receive Data to enter the Assembly Register and since pin 9 of Loop Enable ff is now low, data from Disassembly Register is blocked from passing through gate A1 pin 11. After the word input is complete and Assembly Register cleared, gate B2 pin 12 will again apply a preset to pin 13 of Loop Enable ff. In addition to the receive Start Bit condition described above, the Loop Enable ff is set during another condition. This occurs via gate B2 pin 8 when Half Duplex is not operational (in this case, Full Duplex otherwise called Echo Plex is the interface operating mode), Local is absent (this allows transmission to modem), and a Print Block transfer is not in process. The resulting logic low from gate B2 pin 8 force sets Loop Enable ff. Again, the Assembly Register now loads only from the remote interface. In this condition, any keyboard data entries will leave the Disassembly Register as Send Data via gate A3 pin 6 thence to the modem via driver D10 pin 6. No Send Data will pass to Assembly Register for internal action and/or storage. Only if received back from remote equipment will displayable keyboard data entries enter the Assembly Register. Pursuant to refresh memory storage and display note that local or printer block transfer operational modes always hold the output of gate A3 pin 6 logical high thus holding driver D10 pin 6 output (Diagram 100) at a logical 1 (~3 volts minimum, marking). Without local or block transfer, serial send data may be sent beginning with a logic high start bit from gate A1 pin 6 which allows Send Data from gate A3 pin 6. Send Data applied to driver D10 pin 4 enables Start Bit output from pin 6 (more positive than +3 volts, spacing).

DISASSEMBLY REGISTER (B6/B7) — Parallel data word bits from keyboard or display refresh memory enter the Disassembly Register via the Data Control gates (Diagram 104) when the parallel enable signal is present on pin 9 of each 4-bit register (B6 and B7). This happens in only one of two ways: 1) Keyboard input data is enabled, or 2) Read Memory occurs during a Printer Block Transfer operation (see gate C3 pin 3, Diagram 101).

KEYBOARD STROBE SIGNAL (pin 9, C4) — Keyboard strobe is a control signal which enables keyboard data codes to enter the logic module. Strobe signal occurs when a data entry or data control key is pressed on a data entry keyboard associated with the logic module. If print block transfer operation is not active, this signal passes through gates C4 pin 8, and D6 pin 6. Break signal from keyboard will also initiate a strobe signal via gate D6 pin 6 when print block transfer is not active. Keyboard Strobe Enabled signal (gate A3 pin 8) is produced as a result of a Strobe signal combining with Local or Clear to send signals when the Disassembly Register is not active. The Keyboard Strobe Enabled enables the start bit for the forthcoming keyboard data code (see gate C3 pin 11, Diagram 101). When the keyboard input is not a Break, this signal also generates the signal Keyboard Data Enabled from gate B10 pin 11 before Start Bit ff B3 pin 7 issues the Start Bit signal. The Keyboard Data Enabled signal generates the Parallel Enable signal (gate C7 pin 4, Diagram 101) to load the keyboard data code in the Disassembly Register.

KEYBOARD DISABLE SWITCH CIRCUIT — Keyboard Disabled signal from J4-33 holds a logic low disable on the keyboard strobe, disassembly active (ff B3 pin 15), and break active (gate D7, pin 2, Diagram 103) thus preventing any keyboard data input.

LOCAL SWITCH CIRCUIT — Local signal from J4-30 disables data set interface transmission circuits but allows internal data storage from data codes received from keyboard or received from data set interface. Local allows keyboard strobe via gate A3 pin 11. This is for local keyboard data input and display memory storage. Local disables: 1) Request to send via gate B2 pin 5, 2) Break via gate D7 pin 2 (Diagram 103), 3) Send Data by holding gate A3 pin 3 constantly low, and 4) External Loop Enable via gate B2 pin 11.

DISASSEMBLY ACTIVE FF (B3) — The Disassembly Active ff sets after the Start Bit ff is set indicating presence of a data word Start Bit (ff B3 pin 7). Start Bit presets Disassembly Active ff B3 pin 13. At the end of the following transmit sync, Disassembly Active ff sets. The ff remains set until Enable Clear Disassembly Active signal preclears it at pin 14 to start a repeat sequence (see gate D8 pin 8, Diagram 103).

START BIT FF (B3) — Start Bit ff supplies the start bit for data codes derived from either the data entry keyboard or from display memory. Enable Start Bit signal presets pin 2 and when Transmit Sync goes logic high, the ff sets providing a logic low from pin 7. Since pin 7 is tied to pin 3 for a preset clear, the next Transmit Sync low to high transition clears the start bit.

CURSOR CONTROL

DIAGRAM 103

CURSOR UP FF (pin 11, C8) — Cursor Up signal from ff C8 pin 11 combines with a Cursor Up function translation (Diagram 302) to produce cursor up control signal to Basic Control, (gate C3, pin 13). If a Read Memory operation is active, Cursor Up and T4 combine at gate D7 pin 6 to issue the Clear Clear Memory signal. This results in a force clear of ff K4 at pin 15 (Diagram 007). The Cursor Up ff is set by the Clear Input Buffer signal after a clear or a reset function translation has supplied an enable to gate D6 pin 12 via setting ff D6 pin 3. After Read Memory and T4 produces Clear Clear Memory (gate D7 pin 6), the following T3 clears Cursor Up ff C8 on pin 5. Master Clear also clears these ff's.

BREAK ACTIVE SIGNAL — A master clear will force set D9 at pin 11. A signal from A3 will preset D9. When XMIT Sync goes logic high, pin 10 of D9 will go to a logic high. When the logical operating mode is not active and the keyboard is not disabled (J4-33, Diagram 102), then a break signal from the keyboard Break key will be gated through D7 pin 12 to C5 where Keyboard Strobe Enable will gate the signal to pin 13 of D9 causing a preclear. A logic high on XMIT Sync will clear D9 causing pin 10 to go low for a Break Active output. Break Active passes to remote interface via driver D10 pin 6 (Diagram 100). Break Active disables Keyboard Data Enabled (gate A1 pin 13, Diagram 102) but does enable Keyboard Strobe Enable signal via gates C5 and D6 (Diagram 102) if a Printer Block Transfer is not locking out Break/Active at gate D6, pin 5. Besides providing an enable for Keyboard Strobe, the output of gate D6 pin 6 generates a send request by gates A1/A1 (Diagram 103) and also holds Disassembly Register active until the break key is released. It does this by holding gate D4 pin 8 (Diagram 103) logic low. Send request generated by Break generates Request to Send from gate D2 pin 6 (Diagram 102) when the local operating modes is not active. This signal alerts data set communications equipment to the Break on the Send Data line (Diagram 100).

CLEAR DISASSEMBLY ACTIVE SIGNAL (pin 8) — For disassembly of memory or keyboard parallel data codes, gate D4 pin 8 clears the Disassembly Active ff (B3, Diagram 102) at the end of the disassembly operation (after the parity bit and two stop bits). The Up Binary Counter (C10) counts Transmit Sync's which are shifting data bits out of the Disassembly Register. It does not begin counting until Disassembly Active ff (Diagram 102) is set to remove Master Reset from counter pin 1. When the counter output reaches 10₁₀ (Q1 from pin 13 = logical 1 and Q3 from pin 11 = logical 1), and if the Repeat signal from keyboard is not present, then gate C9 is satisfied. This signal stops the counter and satisfies conditions for gate D4. When the input data key on an associated keyboard is released and if no printer Block Transfer operation is in progress, input pin 10 of gate D4 is satisfied, and the output from pin 8 force clears the Disassembly Active ff on Diagram 102.

ENABLE CLEAR DISASSEMBLY ACTIVE SIGNAL (pin 8, D8) — For disassembly of repeated code entries from the associated keyboard, a "time stretching" circuit is required to properly synchronize clearing the Disassembly Active ff in coordination with the baud rate selected for transmission. When repeat signal is present (from J4-28), Clear Disassembly Active via gates C9, C8, and D4 is disabled. Repeat and a count of 8₁₀ (Q3 pin 11 = logical "1") enables gate D7 output pin 8. This signal applies an enable to gates C8 pin 2, D8 pin 4, and D8 pin 1. If transfer baud rate is 75 or 110 baud, gate C8 pin 3 allows Enable Clear Disassembly Active via gate D8 pin 8. When 300 baud is active, terminal count from counter pin 15 presets pin 2 of ff D9. When this ff sets, it represents a count of 16₁₀. This count combines with an additional count of 12₁₀ at gate D8 to produce the clear.



PRINTER CONTROL AND DATA CONTROL
DIAGRAM 104

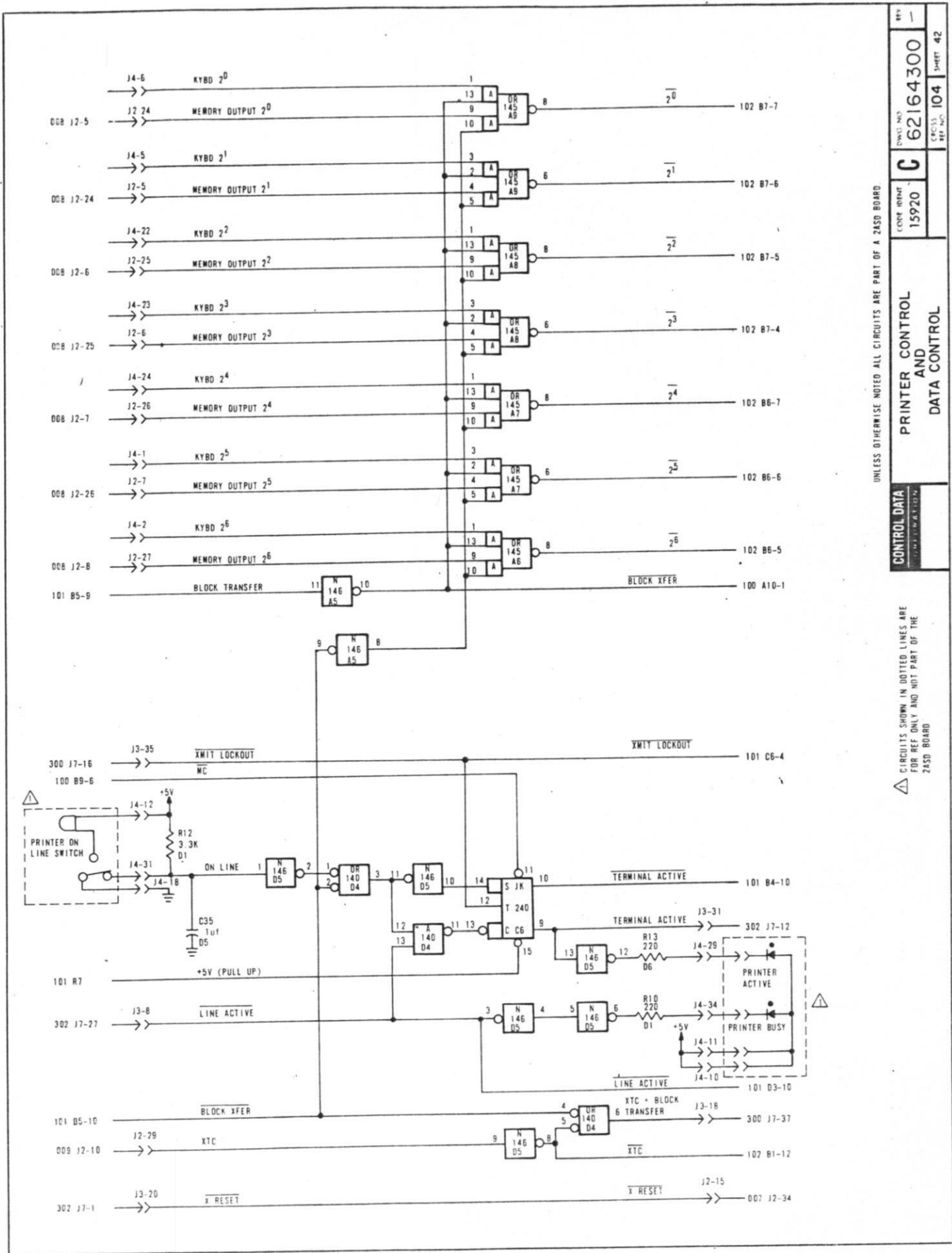
DATA CONTROL GATES (A6 through A9) — These gates are Dual 2-2 Input type which allow either keyboard data codes or memory output data codes to pass to the Disassembly Register (Diagram 102). A printer Block Transfer function (Diagram 101 ff B5) prevents keyboard data codes and allows Memory Output data codes. When printer Block Transfer is not active, keyboard data is allowed and memory codes are inhibited. These data control gates are necessary to let the one Disassembly Register accept and serialize either memory data words for block transmit to an associated printer, or to accept keyboard data entry codes.

ON LINE SIGNAL (pin 1, D5) — The On Line signal initiates conditions to transfer all Receive Data or Send Data to the printer channel. This provides for hardcopy record of received or transmitted messages as they occur data-word-by-data-word. On Line and printer line not active (printer channel not in use by any associated display terminal including the one housing the logic module) satisfies gate D4. This presets Terminal Active ff C6 at pin 13. When transmit lockout signal goes high (at the end of T5) ff C6 toggles to provide Terminal Active signal from pin 9 and Terminal Active from pin 10. As long as the On Line signal is preset at gate D5 pin 1, the logic module will now remain active with an associated printer. Block transfer operation will also cause a Terminal Active condition via gate D4 pin 2 but only for the duration of the print key initiated Block Transfer (see Block Transfer ff, Diagram 101).

TERMINAL ACTIVE FF (pins 9 and 10, C6) — Terminal Active from pin 9 supplies an enable to the four printer channel drivers shown on Diagram 302. In the case of the Active line driver, A10, the Terminal Active signal applied to input pin 1 causes the driver to place interface outputs pin 12 and pin 13 in the Active signal condition. Any other terminals which may share the printer channel along with the terminal containing this logic module, cannot gain access to the channel as long as this signal is active. The Terminal Active signal from ff C6 pin 9 also enables an associated Printer Active indicator light via inverter D5 pin 12. The complementary signal from ff C6, Terminal Active, prevents a Block Transfer Reset signal from gate B4 pin 8 on Diagram 101. This eliminates the chance of a Printer Block transfer.

LINE ACTIVE SIGNAL (J3-8) — This signal is present when the printer data channel is in use by this equipment or another equipment sharing the channel. This signal prevents this equipment from going active on the channel (ff C6 cannot set). It also enables the Printer Busy indicator circuit. Furthermore, the Line Active signal prevents a block transfer print operation by preventing a preset on Block Transfer ff B5 pin 13 (Diagram 101).

XTC + BLOCK TRANSFER SIGNAL (pin 6, D4) — Either X Terminal Count from Diagram 009 (one scan line complete and scan beam back at X Counter = 0) or print block transfer ff set (Diagram 101) will enable gate D4 output pin 6. This signal is used to control Remote Loop Enable ff B1 (Diagram 102) and Clear Active 2 signal at gate D7 (Diagram 301). This signal also enables Receive Timing (Diagrams 300, 301, and 302).



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 2450 BOARD

REV	1
DWG NO	62164300
C	15920
CRCS	104
REF NO	SHEET 42
CONTROL DATA	PRINTER CONTROL AND DATA CONTROL

△ CIRCUITS SHOWN IN DOTTED LINES ARE FOR REF ONLY AND NOT PART OF THE 2450 BOARD

CONNECTOR J1	
NO	SIGNAL
1	+5V
2	
3	+12V
4	-12V
5	GROUND
6	(KEYED PIN)
7	
8	+12V
9	-12V
10	GROUND

CONNECTOR J2	
NO	SIGNAL
1	T4
2	T3
3	
4	
5	MEMORY OUTPUT 21
6	MEMORY OUTPUT 23
7	MEMORY OUTPUT 25
8	
9	
10	T8
11	CURSOR X 26
12	CURSOR X 21
13	
14	X RESET
15	COUNT UP
16	CURSOR X 23
17	BLINK T. C.
18	
19	
20	CLEAR CLEAR MEMORY "
21	TOP LINE
22	
23	
24	MEMORY OUTPUT 20
25	MEMORY OUTPUT 22
26	MEMORY OUTPUT 24
27	MEMORY OUTPUT 26
28	
29	XC
30	
31	CURSOR X 22
32	CURSOR X 20
33	T5
34	
35	
36	MC
37	
38	T1

CONNECTOR J3	
NO	SIGNAL
1	SEND DATA
2	REQUEST TO SEND
3	RECEIVE DATA
4	CLEAR TO SEND
5	DATA SET READY
6	HALF DUPLEX
7	BUSY 2
8	LINE ACTIVE
9	ENABLE BRK
10	300 + 75 BAUD
11	MC
12	CLEAR ASSEMBLY REG
13	CURSOR UP
14	CONT BRK • ENABLE BRK
15	T1
16	BLOCK TRANSFER RESET
17	XMIT SYNC
18	XC + BLOCK TRANSFER
19	BREAK ACTIVE
20	X RESET
21	DATA TERMINAL READY
22	110 + 75 BAUD
23	CLEAR + RESET
24	SCROLL DISABLE
25	T5
26	LOOP ENABLE
27	RING BELL
28	BLOCK TRANSFER
29	EVEN
30	ODD
31	TERMINAL ACTIVE
32	CONTINUOUS DTR
33	CLEAR ACTIVE 2
34	READ MEMORY
35	XMIT LOCKOUT
36	SET P. E.
37	CLEAR INPUT BUFFER
38	RECEIVE DATA + TRANS DATA

CONNECTOR J4	
NO	SIGNAL
1	KYBD 25
2	KYBD 26
3	DATA SET READ
4	CLEAR TO SEND
5	KYBD 21
6	KYBD 20
7	
8	
9	+5V
10	+5V
11	+5V
12	+5V
13	+5V
14	+5V
15	+5V
16	GROUND
17	GROUND
18	GROUND
19	GROUND
20	
21	
22	KYBD 22
23	KYBD 23
24	KYBD 24
25	
26	X
27	ALARM
28	REPEAT
29	PRINTER ACTIVE
30	LOCAL
31	ON LINE
32	BREAK
33	KYBD DISABLE
34	PRINTER BUSY
35	DISABLE SCROLL
36	STROBE
37	PRINT KEY
38	PARITY

CONNECTOR J5	
NO	SIGNAL
1	
2	
3	
4	
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CONNECTOR J6	
NO	SIGNAL
1	
2	
3	
4	
5	
6	
7	
8	
9	
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CONTROL DATA
IDENTIFICATIONSIGNAL IDENTIFIER SHEET
2 ASD BOARDCODE IDENT
15920

C

DWG NO
62164300CROSS
REF NO

SHEET 43

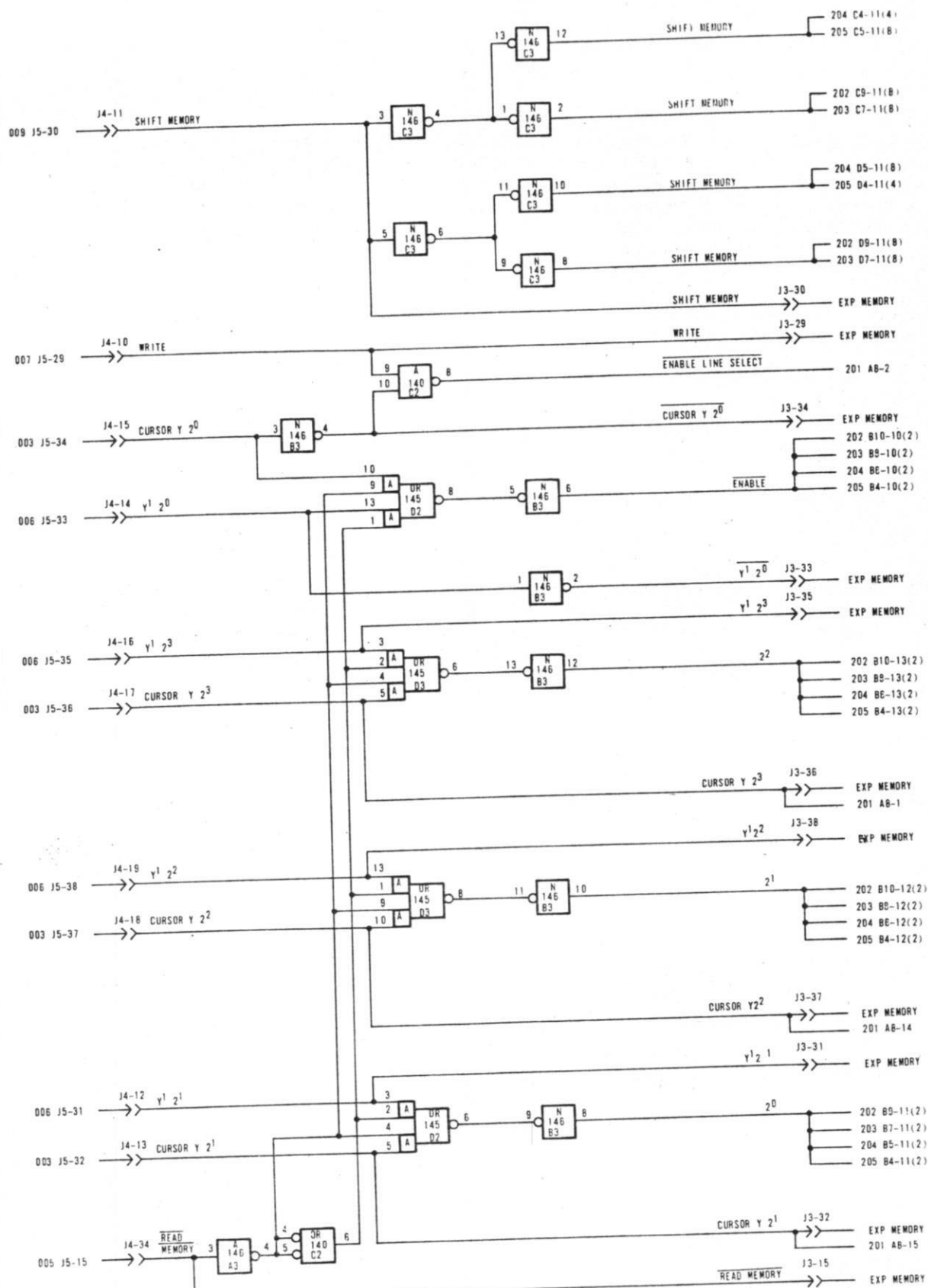
BASIC MEMORY CONTROL 8 LINES

DIAGRAM 200

OUTPUT MEMORY LINE SELECTION — During a refresh, the memory line selection is determined by the $Y'2^0$, $Y'2^1$, $Y'2^2$, $Y'2^3$ lines coming into gates D2/D2, D3/D3. The Read Memory input is at a logical 1, enabling the gating of the Y' signals. These signals go to Read Line Select B10 (Diagram 202) to provide selection of the Quad-80 read/write memory.

INPUT MEMORY LINE SELECTION — During memory operation, other than refresh, the memory readout occurs at the present location of the cursor. Cursor location is determined by Cursor $Y2^0$ to 2^3 . These input lines are gated through D2/D2, D3/D3 when an X-compare (Diagram 005) causes the Read Memory signal to go to logical 0. These signals are gated to Read Line select the same as the Y' signal. For a write operation, the Cursor $Y2^0$ is gated by C2 when a Write signal is on pin 9, C2, and Cursor $Y2^0$ = logical 0. If Cursor $Y2^0$ is logical 1, it will not gate through C2, but will go to the expanded memory, if present. The Enable Line Select from C2 pin 8 enables the Write Line Select A8 (Diagram 201).

SHIFT MEMORY DRIVERS — The circuits C3 provide expansion for the Shift Memory pulse from F9 (Diagram 009). During a memory write or read, the Shift Memory signal goes low with the leading edge of T4 (Diagram 009). Outputs from C3 go to the shift registers of the Quad-80 memory to shift the next symbol code forward to the memory output lines. Shift pulses occur during display time only (X counter = 0 through X counter = 79_{10}).



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A DIB BOARD

CONTROL DATA
CORPORATION

BASIC
MEMORY CONTROL
8 LINES

CODE IDENT
15920

DWG NO
C

62164300

REV
1

CROSS
REF NO
200

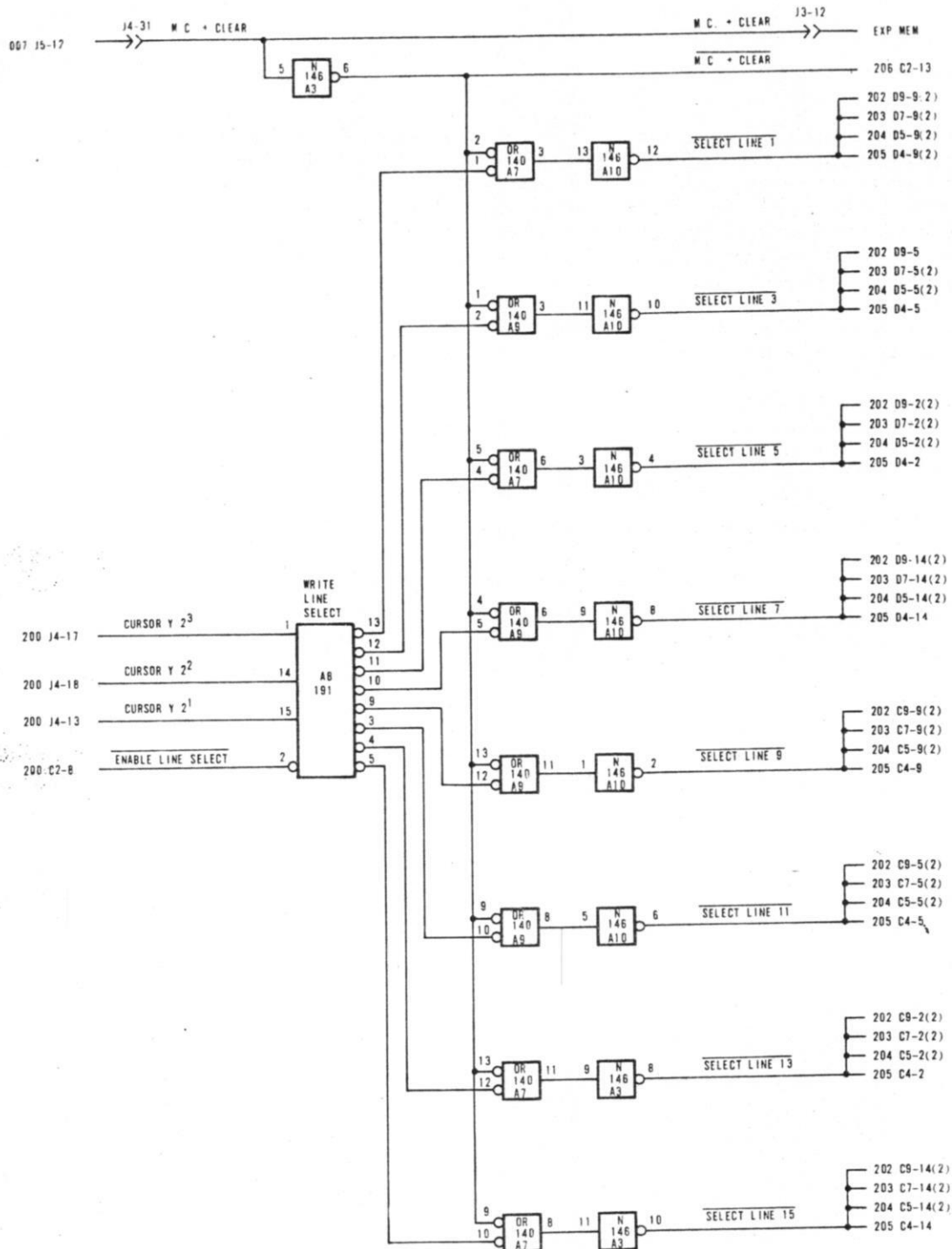
SHEET
44

MEMORY INPUT
DIAGRAM 201

WRITE LINE SELECT (A8) — During data entry, the Write Line Select 1-of-8 selects the line in memory which contains the cursor. If the Cursor Y Counter contains an even count (Bit 2^0 = logical 0), an X Compare produces the Enable Line Select signal for the basic memory. If the count is odd, the optional Expanded Memory Kit receives the Enable Line Select signal. This line is now a logical 0 which allows the decoder to use the count in the Cursor Y Counter to select the memory line which contains the cursor. Cursor Y Counter output which places a logical 0 on one of the decoder output pins is

CURSOR Y COUNTER			OUTPUT PIN SELECTED
2^3	2^2	2^1	
0	0	0	13
1	0	0	12
0	1	0	11
1	1	0	10
0	0	1	9
1	0	1	3
0	1	1	4
1	1	1	5

ENABLE ALL LINES — To clear the read/write memory, the Master Clear or Clear ff (pin 12 of H2/H3, Diagram 007) sends the Enable All Lines signal to simultaneously enable the inputs of all the lines in memory. With all inputs enabled, the Clear Memory ff (pin 6 of K2, Diagram 007) forces Space codes at the inputs to the memory. Each Shift Memory pulse C3 (Diagram 200) loads a Space code in each memory line. After 80 Shift Memory pulses, the memory is filled with Space codes and all the data has been erased from the display screen.



NOTE BASIC MEMORY DISPLAYS DATA ON LINE POSITIONS 1 3 5 7 9 11 13 15₁₀
 EXPANDED MEMORY WILL DISPLAY DATA IN LINE POSITIONS 2 4 6 8 10 12 14 16₁₀

UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A QJND BOARD LOCATED AT

REV	62164300	REV 2	201	SHEET 45
CODE IDENT	15920			
CONTROL DATA	MEMORY INPUT			

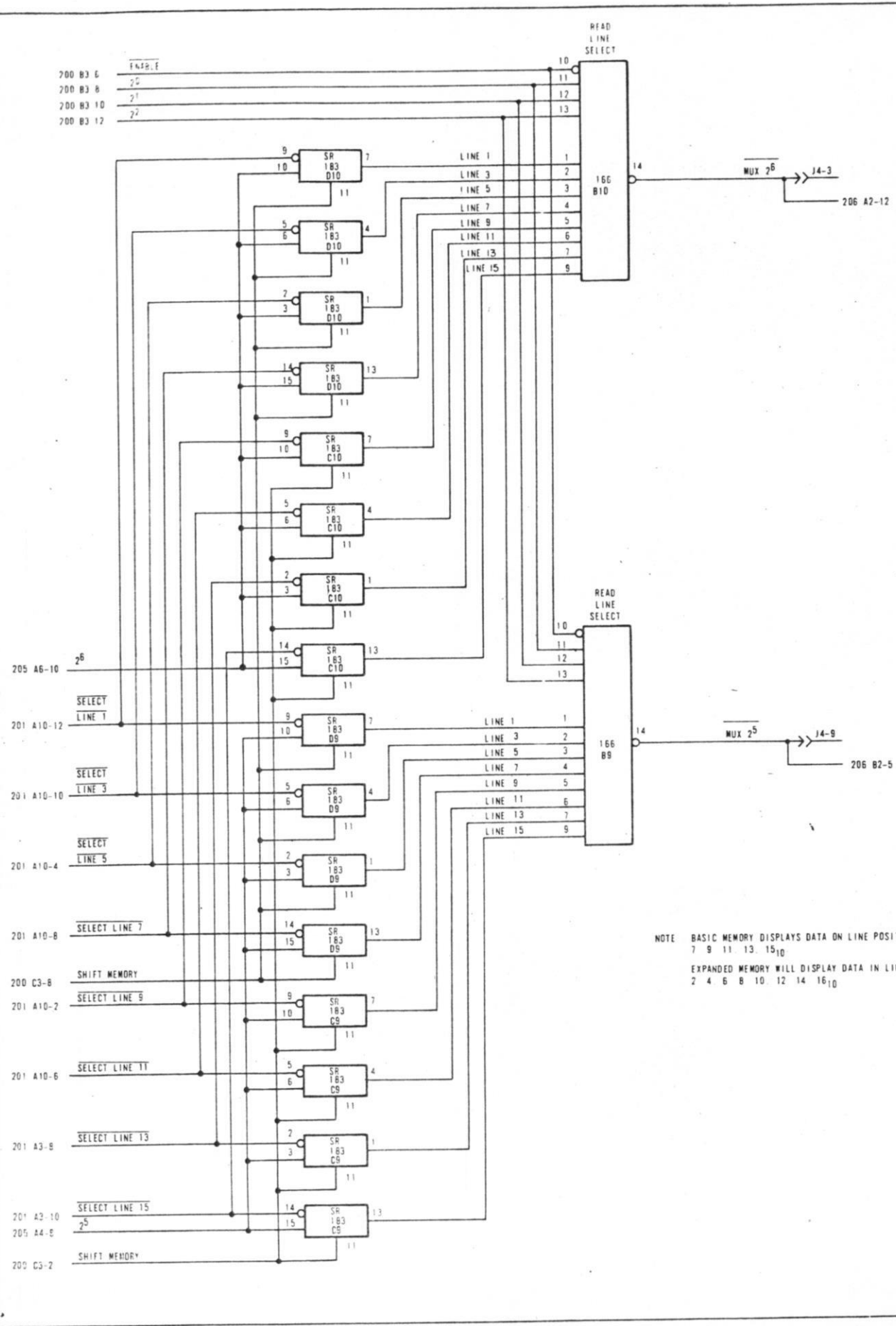
MEMORY MUX 2^5 AND 2^6

DIAGRAM 202

QUAD-80 MEMORY — The Quad-80 memory of the Diagrams 202, 203, 204, and 205 stores 640 7-bit codes. Memory arrangement provides storage for 80 codes for each of eight display lines ($8 \times 80 = 640$). Memory construction uses seven groups of eight memory units (shift registers). The term "memory unit" refers to one logic diagram 80-bit shift register, for example, the shift register D10 with output pin 7 at the top of this diagram. (Because a logic chip contains four 80-bit shift registers, the term "Quad-80" memory is used to refer to the read/write memory.) The term "group" refers to the electrical grouping of eight memory units at the inputs of one Read Line Select multiplexer, for example, B10 at the top of this diagram. The seven separate groups provide for the parallel storage of the 7-bit codes. During the parallel read out of a code, one memory unit in each of the seven groups furnishes one bit of the 7-bit code. Also, this one memory unit supplies all the bits for the same bit position for each of the 80 codes of a specific display line.

READ LINE SELECT — During a refresh, an Output Data, Input Data, or Input Control operation, the Read Line Select 1-of-8 multiplexer selects the memory lines one at a time for the output of the symbol codes stored in that line. The multiplexer inputs $\overline{\text{ENABLE}}$, 2^0 , 2^1 , and 2^2 determine the memory line selection. During a refresh, the Y' Counter supplies the inputs. During the read portion of an Output Data, Input Data, or Input Control function, the Cursor Y Counter supplies the inputs. (Refer also to OUTPUT MEMORY LINE SELECTION, Diagram 200). The coding for the selection of the multiplexer input line is:

2^2	2^1	2^0	$\overline{\text{ENABLE}}$	ENABLED INPUT PIN
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	9

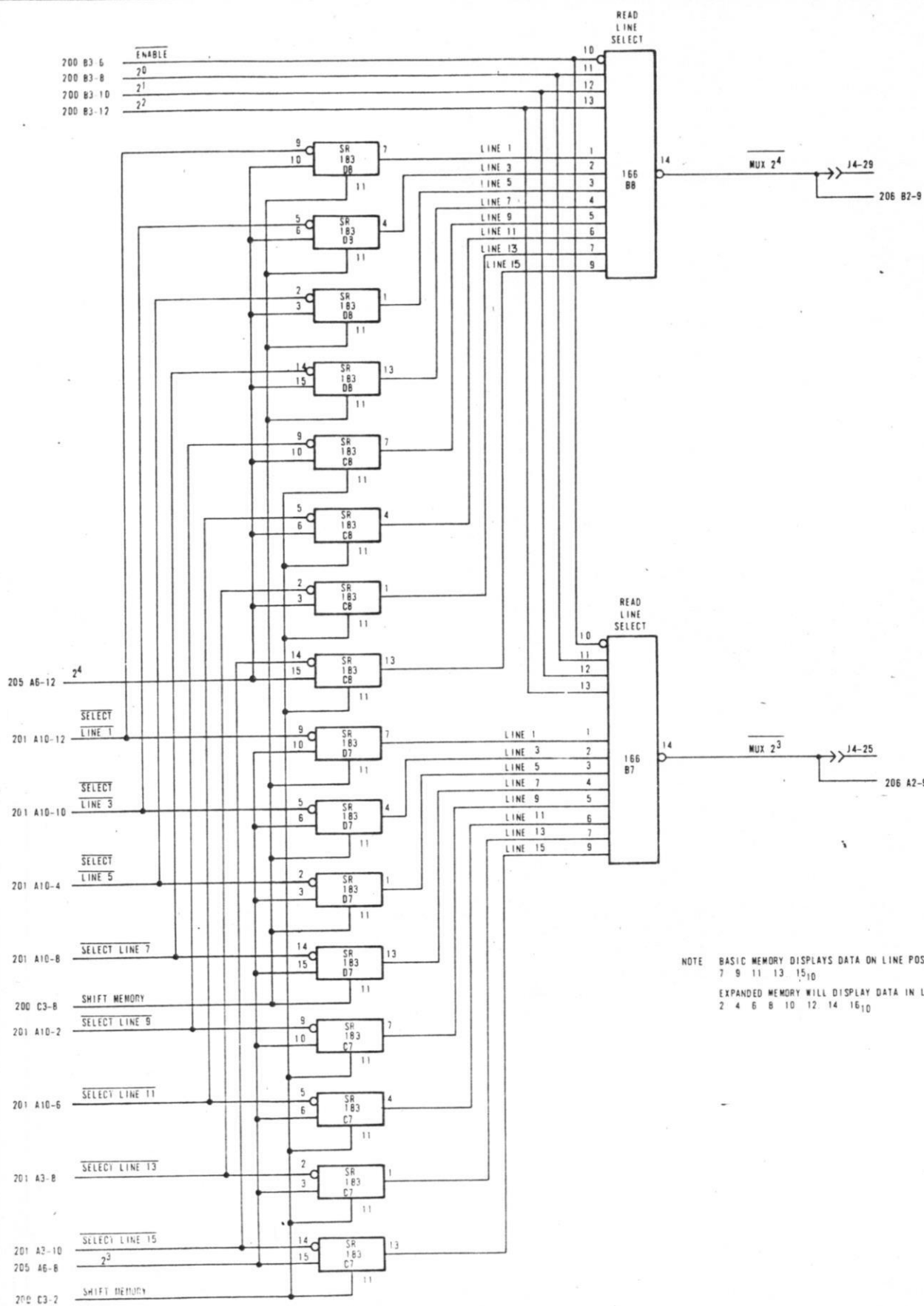


MEMORY MUX 2³ AND 2⁴

DIAGRAM 203

Backup information the same as Diagram 202.

UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF AN DHD BOARD

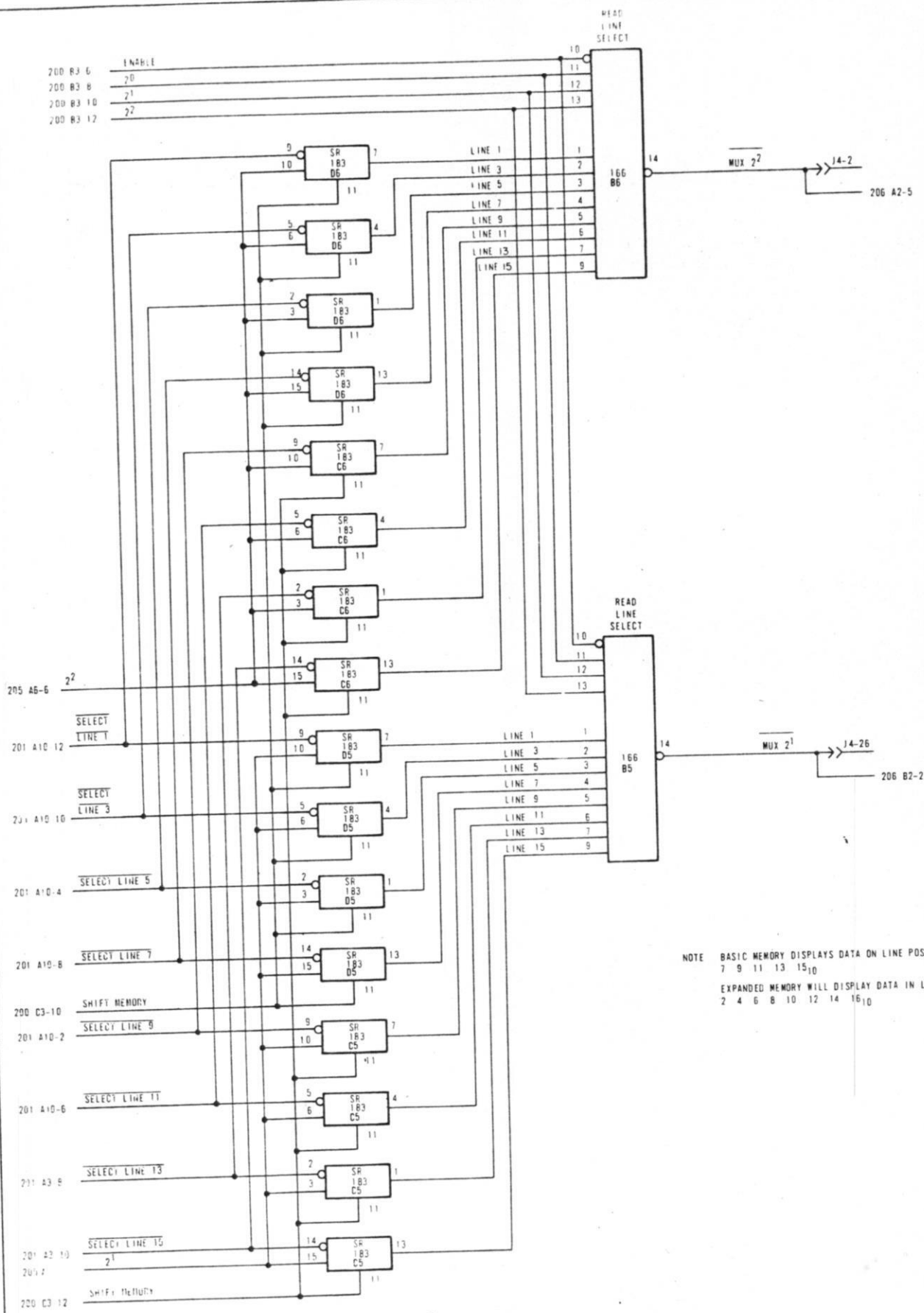


NOTE BASIC MEMORY DISPLAYS DATA ON LINE POSITIONS 1 3 5
7 9 11 13 15
EXPANDED MEMORY WILL DISPLAY DATA IN LINE POSITIONS
2 4 6 8 10 12 14 16

MEMORY MUX 2^1 AND 2^2

DIAGRAM 204

Backup information the same as Diagram 202.



NOTE BASIC MEMORY DISPLAYS DATA ON LINE POSITIONS 1 3 5
7 9 11 13 15₁₀
EXPANDED MEMORY WILL DISPLAY DATA IN LINE POSITIONS
2 4 6 8 10 12 14 16₁₀

UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF AN OJND

REF.	62164300	REV. 204	48
PAGE NO.	C		
CONTROL DATA CORPORATION	MEMORY MUX 2 ¹ & 2 ²		
DATE	15920		

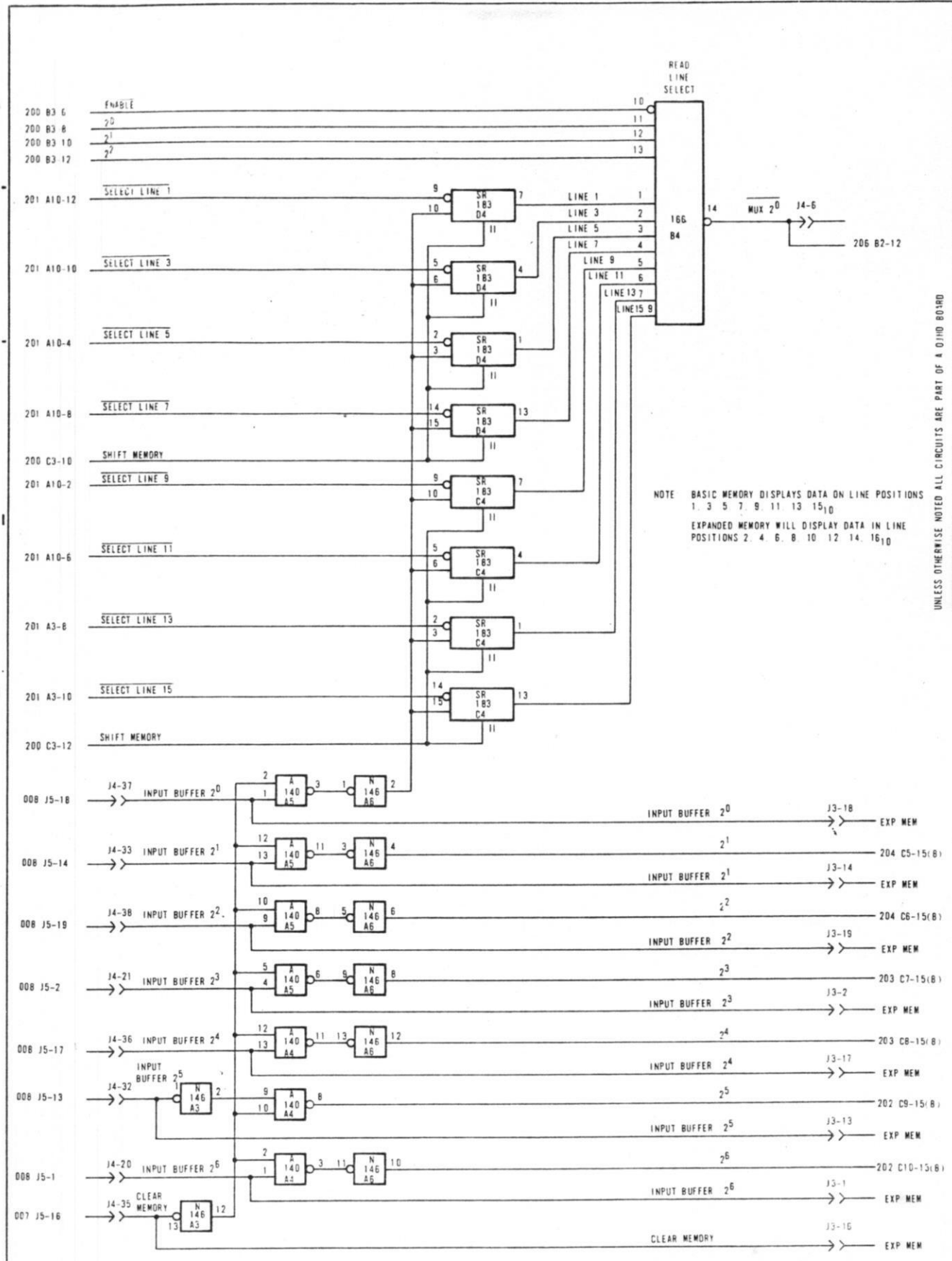
MEMORY MUX 2⁰
DIAGRAM 205

INPUT LINES TO THE QUAD-80 MEMORY — The signal lines Input Buffer 2⁰ through 2⁶ are the 7-bit symbol code input lines to the memory.

CLEAR MEMORY — The Clear Memory signal at pin 13 of gate A3 arrives from the Clear Memory ff (pin 6 of K2. Diagram 007) to force Space codes (040₈) at the inputs of the shift registers.

READ LINE SELECT — See backup page for Diagram 202.

UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 0110 80180

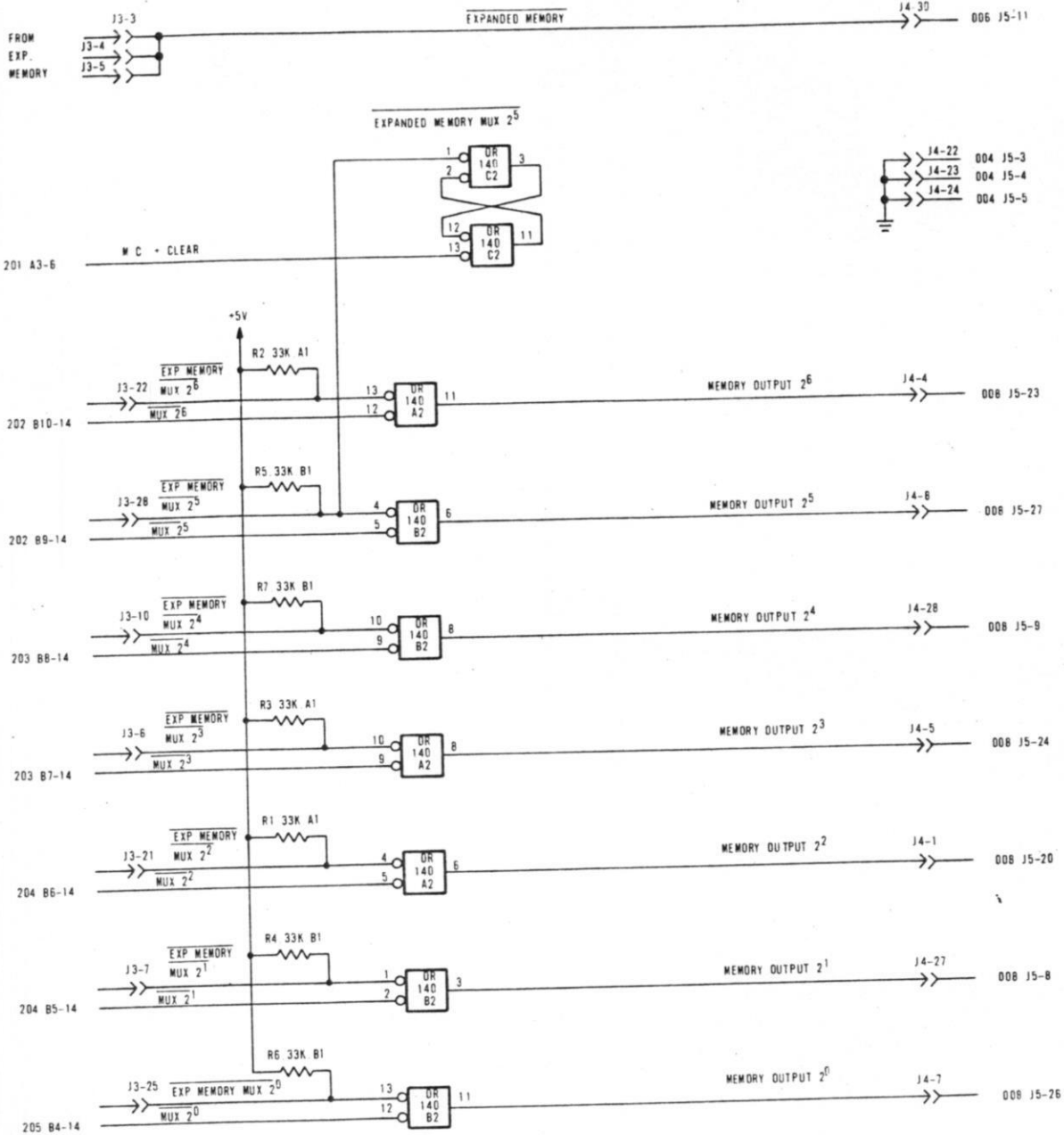


MEMORY OUTPUT

DIAGRAM 206

MEMORY OUTPUT LINES — Both the basic and the optional Expanded Memory Kit multiplexer outputs pass through the OR gates of this circuit to become the outputs Memory 2^0 through 2^6 .

EXPANDED MEMORY FF (C2/C2) — When the optional Expanded Memory Kit is a part of the display station, a master clear first clears the Expanded Memory ff. Then, the memory fills with Space codes (040_8). The 2^5 Bit of one of these Space codes sets this ff. The Expanded Memory line of pin 11 of this ff becomes a logical 0 to block the Cursor Y Clock Pulse which occurs at T1 (pin 12 of K3, Diagram 006). Now, when the cursor advances from display line to display line, it will advance from a basic memory display line to the expanded memory display line which follows, or vice versa. The Expanded Memory signal also prevents an odd count in the Y Counter from direct clearing the White ff (pin 4 of D1, Diagram 005). If a black-on-white display existed at the end of a basic memory display line (no End Tab code detected), this allows the black-on-white display to continue in the display line provided by the expanded memory.



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A DHD BOARD

REV	1
DWG NO	62164300
CODE IDENT	C 15920
CONTROL DATA CORPORATION	MEMORY OUTPUT
206	SHEET 50

TRANSMIT CLOCK

DIAGRAM 300

TIME BASE COUNT gate (C10 pin 6) — On the low to high transition of the output signal from C10, counter D5/D6 (Diagram 300) and C7/C8 (Diagram 301) are incremented. The Time Base Count pulse operates at two different frequencies depending on the input at pin 4 of C10. With Block Transfer signal on the input, pin 4 of C10 (assuming Lockout and Input not present on pins 2 and 1), then the Time Base Clock Pulse is generated each time T3 drops. This occurs every 600 nsec and provides the bit rate for block transfer of information to the printer channel. If Block Transfer is not active, then the Time Base Count Pulse occurs only when the X-Terminal Count (XTC) occurs and T3 drops. XTC occurs once every 63.6 nsec following the X counter return to zero after counting all X positions for a scan line. The Block Transfer pulse occurs 106 times for each XTC pulse.

TIME BASE COUNTER (D5/D6) — This counter and the Baud rate control signals produce the control for timing the Transmit Sync signal. The two cascaded counters D5, D6 operate as ring counters synchronous with the low to high transition of the Time Base Count pulse at input pin 2 of each counter. Initial counting starts when pin 15 of D6 is high causing a logic low at pin 9 of D5 and D6 enabling a parallel loading or preset of D5 and D6 at time T3 from Time Base Count gate C10. The preset count is determined by the Baud rate switch, shown in the upper left of Diagram 300. This is a five position switch with Baud rates as follows: 1) 75 baud, 2) 110 baud, 3) 150 baud, 4) 200 baud (not marked on diagram, contact is open as shown), 5) 300 baud. Selection of a baud rate places a logic low (ground) on the selected position (if it is not 200 baud) and leaves the others at logic high. The combination of these logic levels with gates D8, D9, and D10 provide a preset count on pins 3, 4, 5, and 6 of D5 and 3, 4, and 5 of D6. Pin 6 of D6 is always at logic high. Count Enable Trickle pin 10 of D5 is always logic high allowing the Time Base Count pulses to increment D5. When pin 15 of D5 places a logic high on Count Enable Trickle pin 10 of D6, then the Time Base Count pulse advances D6.

The Transmit Clock Loading table shows the binary input used to preset D5 and D6. The logical 1 represents a logic high input. Preload is performed when pin 9 is low, pin 15 of D6 high.

TRANSMIT CLOCK LOADING

Gate/Pin	D5/3	D5/4	D5/5	D5/6	D6/3	D6/4	D6/5	D6/6
Baud Rate								
300	0	1	1	0	0	1	1	1
200	1	0	0	1	1	0	1	1
150	0	0	1	1	0	0	1	1
110	1	0	0	1	1	1	0	1
75	1	1	1	0	1	0	0	1

The difference between a full count (256) and the preset count is the number of Time Base Count pulses required between each half bit time. This means the Time Base Counters (D5, D6) must perform two full counts for each Xmit Sync pulse. Pin 15 of D6 toggles ff B7 on each output. The second full count of D5/D6 will place pin 10 of B7 at a logic high enabling D3 at pin 5.

The Transmit Frequency table lists the transmit times for each baud rate for XTC Clock times and Block Transfer Clock times.

TRANSMIT CLOCK
DIAGRAM 300 (CONT)

TRANSMIT FREQUENCY

BAUD RATE	LOAD COUNT	HALF CYCLE COUNT	HALF CYCLE LOAD COUNT	XMIT COUNT	XTC TIME	XTC XMIT CLOCK TIME	BLOCK TRANSFER TIME	BLOCK TRANSFER CLOCK TIME
300	230	256	26	52	63.6 μ sec	3.3msec	600nsec	31.2 μ sec
200	217	256	39	78	63.6 μ sec	4.8msec	600nsec	28.8 μ sec
150	204	256	52	104	63.6 μ sec	6.6msec	600nsec	62.4 μ sec
110	185	256	72	144	63.6 μ sec	9.16msec	600nsec	86.4 μ sec
75	151	256	104	208	63.6 μ sec	13.34msec	600nsec	124.8 μ sec

XMIT SYNC (D3) — The Xmit Sync pulse provides timing for circuits involved in the transmission of data from the terminal. Pulse timing from D3 pin 6 is controlled by the Time Base Counter (D5/D6) and T1 on pin 1. FF D2/D2 turns off gate D3 at time T5 to prevent more than one pulse gating through D3.

XMIT LOCKOUT (A7) — Control for Xmit Lockout comes from D2 pin 3 and T5. When both signals are at a logic high, a logic low outputs from A7 pin 6. This signal is at the same rate as the Xmit Sync.

MASTER CLEAR (D7) — The master clear circuit D7 generates complementary output pulses on pins 13 and 4. The output pulse width is a function of the circuit at pins 14 and 15. The master clear switch S4 is mounted on the edge of the circuit board ICGE. Closing this switch discharges capacitor C4 causing the input at pin 1 to go from logic high to logic low producing complementary pulses on pins 13 and 4. A second master clear method is turning off the AC power to the terminal. Power should not be reapplied for 30 seconds to allow capacitor C4 to discharge. Turning on the terminal will cause pin 2 to be high and pin 1 to increase as C4 recharges. This causes D7 to generate complementary output pulses at pins 13 and 4.

RECEIVE CLOCK

DIAGRAM 301

RECEIVE TIME BASE COUNTER (C7/C8) — This counter and associated circuits operate with the Baud rate circuits to produce the Receive Sync signal (gate B9 pin 6) at the proper bit rate to match the sending equipment data bits. Prior to receiving data, ff D4 is clear holding pin 6 low. This clears ff B7 and holds an enable signal, logic low on pin 9 of C7 and C8. The enable allows C7 and C8 to be preset by the Baud rate circuits (Diagram 300) and prevents counters C7/C8 from counting from this preset value.

When a Receive Data or Xmit Data signal is received, pin 3 of C4 goes low placing a logic high on pin 2 ff D4. During data input, pin 3 ff D4 is high. This causes ff D4 to set when XTC or Block Transfer and T3 are present on pin 4. When ff D4 sets, pin 6 goes high allowing counter C7/C8 to increment with the Time Base Count pin 2, at a full count, pin 15 C7 goes to a logic high enabling gate B9 to generate a Receive Sync signal at time T1. Pin 15 of C7 is also gated to pin 9 of C7 and C8 resetting them and allowing a new count to start. When a full count is obtained in C7/C8, ff B7 toggles making pin 6 low and resetting C7/C8 by enabling pin 9. Two full counts are required of C7/C8 for each bit time. The Receive Sync signal occurs at the center of each received data bit.

RECEIVE SYNC SIGNAL (B9, pin 6) — Each Receive Sync pulse shifts a data bit into the Assembly Register (B2/B3, Diagram 303). For received data from the data set interface, Receive Sync will occur 300, 200, 150, 110, or 75 times per second depending on which Baud Rate control signal was selected (Diagram 300). During Block Transfer operation, however, data bits routed through the Assembly Register for write back into refresh memory are sequenced 106 times faster than data received from the data interface. Receive Sync signal and T1 set Resync ff A8/A8. The set condition of pin 11 combines with T5 to set Disable Receive Sync ff A8/A8. The output of this ff from pin 6 applies a logic low disable signal to input pin 5 of Receive Sync gate B9. This terminates Receive Sync signal.

RUN RECEIVE CLOCK (ff D4) — When a receive data input is complete and no Receive Data start bit is present, ff D4 is in the clear condition placing pin 6 at logic low. This holds the Receive Time Base counter in the preset count condition preventing counting with the Time Base Count pulses. A Receive Data Transmit Data start bit applies a logic high preset to pin 2 of the Run Receive Clock, ff D4. The start bit is present for one data bit time. If Block Transfer is active, the Run Receive Clock ff will set at T3. If Block Transfer is not active, the ff sets at T3 when X Terminal Count (XTC) occurs (once per scan line, every 63.6 nsec). With ff D4 set, output pin 6 enables the Receive Time Base Counter and places a Receive Data active signal on pin 9 of gate D3. Normally, the Run Receive Clock ff remains set until after Input Complete applies a preclear on pin 3. This occurs after the last bit of the data word is sequenced. During the following stop bit time, (XTC + Block Transfer) • T3 clears the ff. In addition to the Input Complete Clear, Receive Data ff may be force cleared on pin 1 during any one of four conditions.

- 1) Clear Input Buffer signal because of the end of a control function.
- 2) Clear Active 2 signal (D7 pin 12) is caused if a Loop Enable signal comes in from B1 pin 9 (Diagram 102).
- 3) Clear Active 1 signal (A6 pin 12, Diagram 302) which is caused if the code being sequenced is a no-op function (a function not recognizable by the Function Decoder on Diagram 302).
- 4) If the start bit is no longer present at the half bit count of C7/C8, the Receive Data + Xmit Data line high, then gate D3 will be disabled and gate C5 will be enabled by D4 pin 10 (logic high) and the Receive Data bit. At the half bit time, the output from pin 6 ff B7 will gate through C5 causing ff D4 at pin 1. This will cause pin 6 of ff D4 to go low preventing further counts of C7/C8.

INPUT TIMING AND FUNCTION DECODES DIAGRAM 302

INPUT TIMING FF'S (D1/D1) - These ff's control initiation and termination of data input to display memory. When an input operation is completed, Busy signal becomes a logic low and gate C2 outputs Input Complete signal which preclears ff D1 at pin 13. At the following ending of T5 this ff toggles to output a logic high on pin 9 to end Lockout condition and outputs a logic low from pin 10 to end Input Complete signal. The logic high from pin 9 applies an enable to gate B6 pin 9 so a new input operation can occur. An input will start by either: 1) Set Input at gate B6 pin 13 to initiate storing displayable data codes (040g through 177g), or 2) an input will be for a recognizable function code (displayable functions 003g, 016g, or 017g and operation functions 010g, 012g, 025g, 026g, 030g, 031g, and 032g). For any of these function codes, gate A4 pin 3 issues a logic low which supplies an Input signal to gate B6 pin 12. Either of these two types of input pretoggles Input ff pin 3. At the end of the following T5 this ff toggles to issue Input and Input signals. Input signal disables Input Complete from gate C2 pin 6 and enables Input signal from Exclusive Or gate C3 when Block Transfer Reset signal is not present. Input signal from ff pin 7 places a pretoggle on pin 2 and pin 14 so the next time T5 ends, both ff's set. This terminates Input signal from pin 6 and issues Lockout signal from pin 9. The ff remains in this condition until generation of Input Complete signal.

INPUT COMPLETE signal (pin 6, C2) - Aside from clearing Lockout, this signal initiates clearing the Assembly Register via the Clear Assembly Register ff (D4, Diagram 301).

INPUT signal (Pin 6, D1) - Disables Input Complete signal, enables Input signal to Basic Control (Diagram 007), and prevents a new input by stopping the Time Base Clock Pulse at gate C10 pin 1 (Diagram 300).

LOCKOUT signal (pin 9, D1) - This signal prevents a new input by disabling gate B6 at pin 9 and by stopping the Time Base Clock Pulse at gate C10 pin 2 (Diagram 300).

FUNCTION DECODER (A3) - If Assembly Register data (Diagram 303) is not only in the function data code range (000g through 037g) but also recognized by pretranslation gates (Diagram 303) to be performable by this equipment, then Enable Decoder and Function signals result at Decoder inputs 18 and 19 to gate in the necessary Assembly Register data bits for complete decoding. The functions recognizable by Decoder A3 and associated gates are:

Ring Bell (007g)	Cursor Down (012g)	Reset (025g)	Line Clear (031g)
Backspace (010g)	Skip (025g)	Clear (030g)	Cursor Up (032g)

In addition to these 8 operational functions that the Basic Control (Diagrams 000 through 008) can perform, there are 3 displayable input control function codes:

ETX (003g)	Start Inverse Video (016g)	End Inverse Video (017g)
------------	----------------------------	--------------------------

These codes are recognized as performable via predecoder gate C2 on Diagram 303. Enable Input signal from this gate enables gate A1 at pin 2 the same as display performable function codes do. Any function codes other than those enabling gate A1 to place a logic high at pin 2 of gate A4 will cause Clear Active 1 signal from gate A6 pin 12. Clear Active 1 signal indicates that the Basic Control (Diagrams 000 through 008) is not designed to perform the function in the Assembly Register so the register will be cleared (see gate C5 pin 10 and following circuits on Diagram 301). Note that if Scroll mode is not disabled (gate A4 pin 5) Line Clear function is a no-operation code since gate A4 pin 6 will output logic high. Also note that Ring Bell function need not enable gate A1 pin 8 to be a performable function. It may pass directly to the Ring Bell circuit on interface Diagram 100.

PRINTER INTERFACE DRIVER/RECEIVERS (B10, A9, and A10) - These circuits allow serial data transfer of ASCII 7-bit codes to a receive-only printer device for hardcopy record of either: 1) data stored in display refresh memory (Print Block Transfer operation), 2) data entering the logic module interface from the data set (Printer-on-Line operation), or 3) data entering the logic module interface from an associated keyboard (Printer-on-Line operation).

BUSY 2 SIGNAL (pin 9, B10) - This signal indicates that the associated printer device is busy processing data internally.

TERMINAL ACTIVE SIGNAL (J7-12) - When printer control (ff C6, Diagram 104) supplies this signal, the printer channel becomes available to the logic module. Terminal Active signal places the Active line in a "being used" condition via Driver A10 pin 1. Terminal active enables all 4 drivers by placing a logic high on pin 10.

LINE ACTIVE SIGNAL (pin 4, B10) - This signal is a logic low when the printer channel is in use by this logic module or some other device. Line Active is used by Printer Control (Diagram 104). RECEIVE DATA + TRANSMIT DATA SIGNAL (pin 1, A9) - When Terminal Active signal is logical high, serial data bits for a printer will pass through this driver via this line.

RESYNC SIGNAL (pin 5, A9) - This signal is issued to a printer each time a data bit is stable on the Data Out line. This transmits to the printer as the bit Clock signal. Resync signal is generated by the Receive Clock (Diagram 301) which controls loading the Assembly Register. The reason that this signal is used to clock data to the printer is that all printer channel data is also assembled as Receive Data by the Receive Clock and Assembly Register and the Resync signal time is best for the printer sampling stable data bits on the data line.

DATA WORD ASSEMBLED (pin 5, A10) - This signal is issued to a printer after all 7 bits of a data word have been transferred to the printer on the Data Out line and at the time that the Parity Bit is on the line. This signal transmits to the printer as the word Strobe signal. Data Word Assembled signal is generated from the Assembly Register (Diagram 303). Since data words sent to the printer channel are simultaneously assembled in the Assembly Register, the Data Word Assembled signal time is best for notifying a printer that the data word sent is complete.

ASSEMBLY REGISTER DIAGRAM 303

ASSEMBLY REGISTER (B2/B3) - The Assembly Register converts serial data bits into parallel data words. It receives serial data from the data set interface or from the internal serial-data-to-parallel-data loop for memory storage or function operation (trace Receive Data + Transmit Data signal back to C1 pin 3, Diagram 100; also see Functional Block Diagram shown in figure 4-5). Two cascaded 4-bit Universal Registers compose the Assembly Register. Data enters these registers synchronously with the low to high transition of the Receive Sync signal on pin 10. Data will enter via the first stage J and K inputs (pins 2 and 3 respectively) or each 4-bit register may parallel load by the synchronous Receive Sync when the parallel Enable (pin 9) is logic low due to a Parity Error. When Clear Assembly Register signal places a logic low on pin 1, an overriding Master Reset occurs regardless of the Synchronous Receive Sync signal. Data In 2^0 through Data In 2^6 signals from the Assembly Register supply the Function Decoder (Diagram 302) and the display memory (Diagram 206).

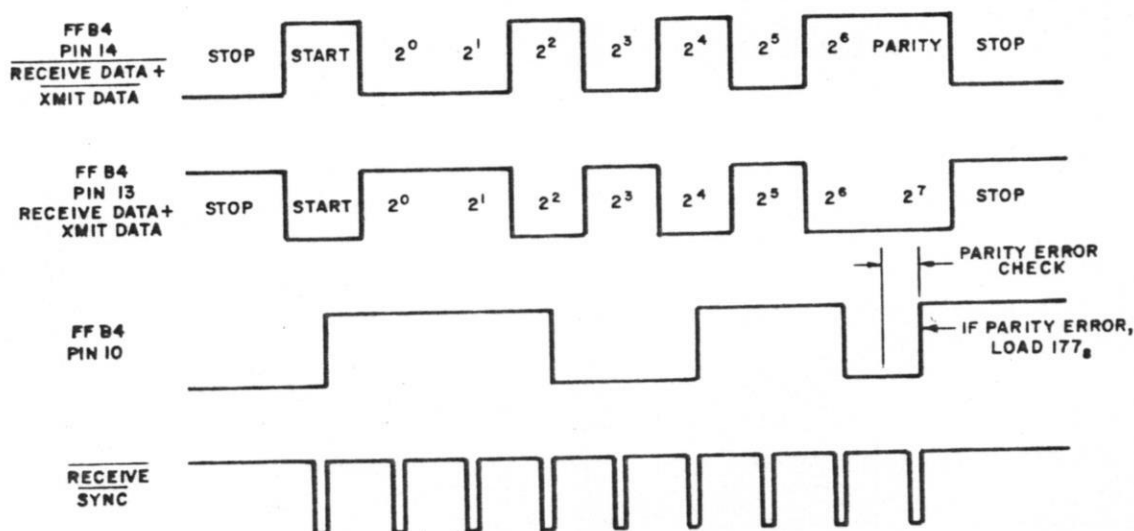
ASSEMBLY REGISTER IN OPERATION - Serial data bits for assembly arrive on the Receive Data + Transmit Data line and input to J and K pins (pins 2 and 3) of register B2. When in the idle or no data state, this line is logic low. When the Start Bit preceding a serial data word arrives, this line becomes logic high. The Receive Clock (Diagram 301) generates Receive Sync signal. When this signal changes from logic low to high, the Start Bit steps into the first stage of 4-bit register B2. This also sets Parity ff B4. The Parity ff keeps track of bit conditions and in conjunction with other circuits (see Parity ff, this page) checks word parity. The least significant data word bit (bit 2^0) follows the Start Bit into register B2 in the same manner as the Start Bit. This shifts the Start Bit one stage up. This entering and shifting process continues until the Start Bit reaches the end or eighth place of the cascaded Assembly Register. At this time, B3 pin 12 issues a logic high which presets Data Word Assembled ff B4 (see Data Word Assembled, this page). The Start Bit logic high also supplies an enable on gate D9 pin 2 for a Parity Error operation if a Parity Error becomes apparent when the Parity Bit now arrives on the Receive Data + Transmit Data lines (see Parity ff, this page). The next Receive Sync low to high transition sets the Data Word Assembled ff (B4) and if no Parity Error is present, shifts the Parity Bit into the Assembly Register. Now B3 pin 11 outputs Data Bit 2^0 , pin 13 outputs Data Bit 2^1 etc. as labeled on the output signal lines. The Start Bit has been shifted out at this point and is no longer in the Assembly Register. If a Parity Error did exist at this last Receive Sync shift time, gate A9 pin 12 would hold a logic low Parallel Enable on page 9 of each register stage and a Parity Error code of 177₈ would load into the Assembly Register.

FUNCTION/FUNCTION SIGNALS - (C1 pin 6 and B1 pin 2) - When the data word is assembled and Resync has ended, bits 2^5 and 2^6 are examined for presence of 1's by gate C1. If neither bit is set, the assembled data word cannot exceed 037₈. Since the function codes used by this equipment are in the range 000₈ through 037₈, if neither bit 2^5 nor 2^6 is set, then Function and Function signals are generated (pins 13 and 14 of B2 each have a logic output).

SET INPUT SIGNAL (A6, pin 8) - If the data word is assembled and it is not a function, when Resync ends gate A6 pin 8 generates the Set Input signal signal to initiate a store data operation (see Diagram 302).

PARITY FF (B4) - The parity ff monitors serial data bits as they enter the Assembly Register. When the start bit reaches B3 pin 12 and the Parity Bit is at pin 5 of gate C3 a decision of correct/incorrect parity is made depending on the setting of the Parity Switch circuit (even, odd, or Mark). See Parity Circuit Operation, this page.

PARITY CIRCUIT OPERATION - An example of assembling a serial code with a specific parity selected follows as a means of explaining Parity Circuit operation. Assume the seven bit code 0101011₂ arrives for parallel assembly and that Even Parity designation accompanies the code (Parity Bit = 0₂). Also assume that the Parity ff is clear as a result of a preceding Clear Assembly Reg signal. Furthermore, the Parity Switch circuit must be set for Even Parity. The following illustration shows how the Parity ff monitors the serial data bits for the code 0101011₂.



ASSEMBLY REGISTER
DIAGRAM 303 (CONT)

The Parity bit places a logic high on pin 5 of Exclusive Or gate C3 and the Parity ff pin 10 is holding a low on pin 4 of the gate. The resulting logic low output at pin 7 disables gate B5 at pin 5. No Parity Error is present. If one of the data bits or the Parity Bit had arrived opposite from intended state, inputs to the Exclusive Or would not be complementary thus pin 7 would place a logic high on gate B5 pin 5. This would load a Parity Error code (177_g) in the Assembly Register when Receive Sync went logic high (see timing illustration).

DATA WORD ASSEMBLED SIGNAL (ff B4, pin 6) - When Start Bit has shifted to the end of the Assembly Register, the following Receive Sync low to high transition causes ff B4 pin 6 to output Data Word Assembled signal. This is the same time when all data bits shift to fill the register (e.g. Data 2⁰ at B3 pin 11) and Start Bit shifted out. This signal allows decoding assembled data word for Function or Input operations.

ENABLE INPUT SIGNAL (C2, pin 8) - This signal is the result of a translation of lower order data bits in the Assembly Register to determine if a storable function (003_g, 016_g, or 017_g) is present. If so, Enable Input will initiate a memory input operation (see Diagram 302).

ENABLE DECODER SIGNAL (B8, pin 12) - This signal is the result of a parity decode of the data word in the Assembly Register to determine if an operable function code exists and if so, Enable Decoder signal combines with the general function indication (Function from gate C1 pin 6) to enable the Function Decoder on Diagram 302.

CONNECTOR J1	
NO	SIGNAL
1	+5V
2	GROUND
3	+12V
4	-12V
5	GROUND
6	(KEYED PIN)
7	+12V
8	-12V
9	GROUND

CONNECTOR J2	
NO	SIGNAL
1	GROUND
2	CLOCK +
3	STROBE +
4	CLOCK -
5	STROBE -
6	CLOCK +
7	DATA OUT -
8	DATA OUT +
9	BUS -
10	BUS +
11	ACTIVE -
12	170 BAUD
13	300 BAUD
14	ACTIVE +
15	GROUND
16	GROUND
17	150 BAUD
18	75 BAUD
19	EVEN
20	ODD
21	CLOCK +
22	STROBE +
23	STROBE -
24	CLOCK -
25	DATA OUT -
26	DATA OUT +
27	BUS -
28	BUS +
29	ACTIVE -
30	DATA TERMINAL READY
31	GROUND
32	HALF DUPLEX
33	DATA SET READY
34	CLEAR TO SEND
35	RECEIVE DATA
36	REO TO SEND
37	SEND DATA
38	GROUND

CONNECTOR J7	
NO	SIGNAL
1	X RESET
2	DATA TERMINAL READY
3	110 + 75 BAUD
4	CLEAR + RESET
5	SCROLL DISABLE
6	15
7	LOOP ENABLE
8	RING BELL
9	BLOCK XFER
10	EVEN
11	ODD
12	TERMINAL ACTIVE
13	CONTINUOUS DTR
14	CLEAR ACTIVE 2
15	READ MEMORY
16	XMIT LOCKOUT
17	SET P.E.
18	CLEAR INPUT BUFFER
19	RECEIVE DATA + XMIT DATA
20	SEND DATA
21	REQ TO SEND
22	RECEIVE DATA
23	CLEAR TO SEND
24	DATA SET READY
25	HALF DUPLEX
26	BUSY 2
27	LINE ACTIVE
28	ENABLE BREAK
29	300 + 75 BAUD
30	MC
31	CLEAR ASSY REG
32	CURSOR UP
33	CONTINUOUS BRK + ENABLE BRK
34	T1
35	BLOCK TRANSFER RESET
36	XMIT SYNC
37	XTC + BLOCK TRANSFER
38	BREAK ACTIVE

CONNECTOR J8	
NO	SIGNAL
1	INPUT BUFFER 2 ⁰
2	INPUT BUFFER 2 ¹
3	INPUT BUFFER 2 ²
4	INPUT BUFFER 2 ³
5	INPUT BUFFER 2 ⁴
6	INPUT BUFFER 2 ⁵
7	13
8	SCROLL DISABLE
9	10
10	11
11	12
12	13
13	14
14	15
15	16
16	17
17	18
18	19
19	20
20	21
21	22
22	23
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26	27
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28	29
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30	31
31	32
32	33
33	34
34	35
35	36
36	37
37	38

CONNECTOR J5	
NO	SIGNAL
1	
2	
3	
4	
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27	
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29	
30	
31	
32	
33	
34	
35	
36	
37	
38	

CONNECTOR J6	
NO	SIGNAL
1	
2	
3	
4	
5	
6	
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CONTROL DATA CORPORATION		SIGNAL IDENTIFIER SHEET		ICGE BOARD		C 62164300		REV 56	
CODE IDENT		15920		C 62164300		REV NO		SHEET 56	

SECTION 6

MAINTENANCE

This section describes maintenance procedures to be used in conjunction with Section 5, Diagrams, Section 7, Maintenance Aids, and Section 8, Parts Data.

PREVENTIVE MAINTENANCE

Preventive maintenance provides a method to maintain the performance and prevent the failure of equipment. When a logic module is returned for repair, the following preventive maintenance procedures should be followed.

1) Cleaning.

- a) Remove power from unit by turning power off.
- b) Vacuum unit thoroughly (do not damage wiring or parts).
- c) Dust panels and hardware with a soft-bristled brush.

2) Visual inspection.

- a) Remove power from unit by turning power off.
- b) Verify all cables and wires are secure and free from insulation breakdown or other damage.
- c) Check all electrical connections for damage or loose connections.
- d) Check for foreign objects such as bits of wire or solder.
- e) Check electronic components for deterioration signs such as overheating.

3) Mechanical inspection.

- a) Verify all electrical connectors are secure.
- b) Verify all printed-circuit cards are seated properly.

4) Operational checks.

Place module in an operational display/keyboard or tester and exercise (see on-site customer engineering manual for module remove/replace procedures and see reference manual for operation and programming). If using a tester, see the tester operation manual.

CORRECTIVE MAINTENANCE

The logic circuits need no adjustment. Because all the logic printed-circuit boards are normally laid out on a flat working surface during maintenance, no special test points or card extenders are needed.

SECTION 7

MAINTENANCE AIDS

This section supplies information to assist in finding the location of a fault. The aids here are symbol formations; waveforms of the horizontal and vertical sync pulses, the eight display lines filled with H's, a full display line of H's, and the first scan line of H's; and a troubleshooting chart.

Figure 7-1 shows the dot pattern of the displayable characters as they appear on the display screen.

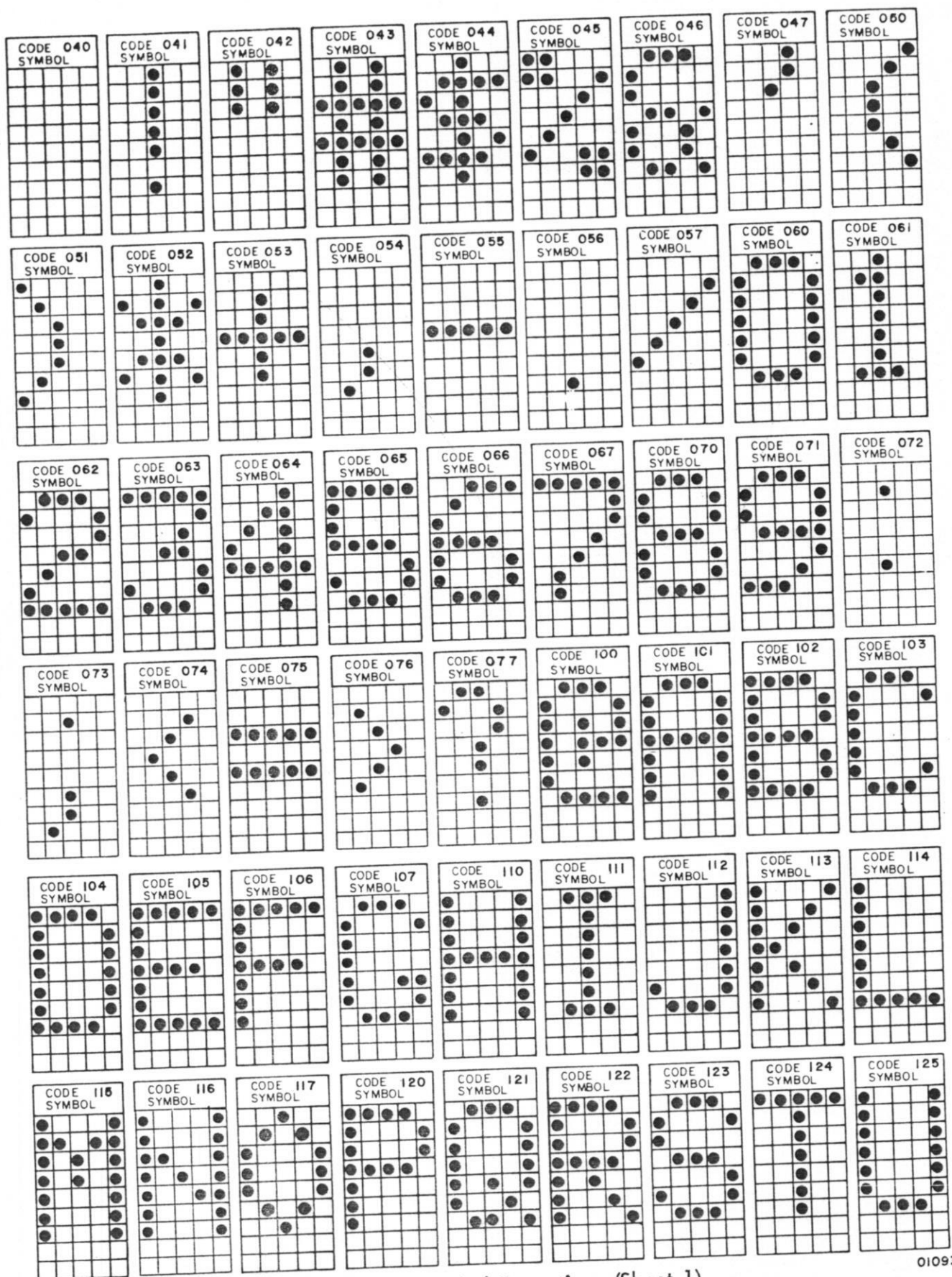
Figure 7-2 shows the sync pulses at the base of K1Q4.

Figure 7-3 shows the eight display lines used to form the character H as seen at the base of K1Q4, Diagram 008.

Figure 7-4 shows the pulses seen at the base of K1Q4, Diagram 008, for the formation of a full display line of the character H.

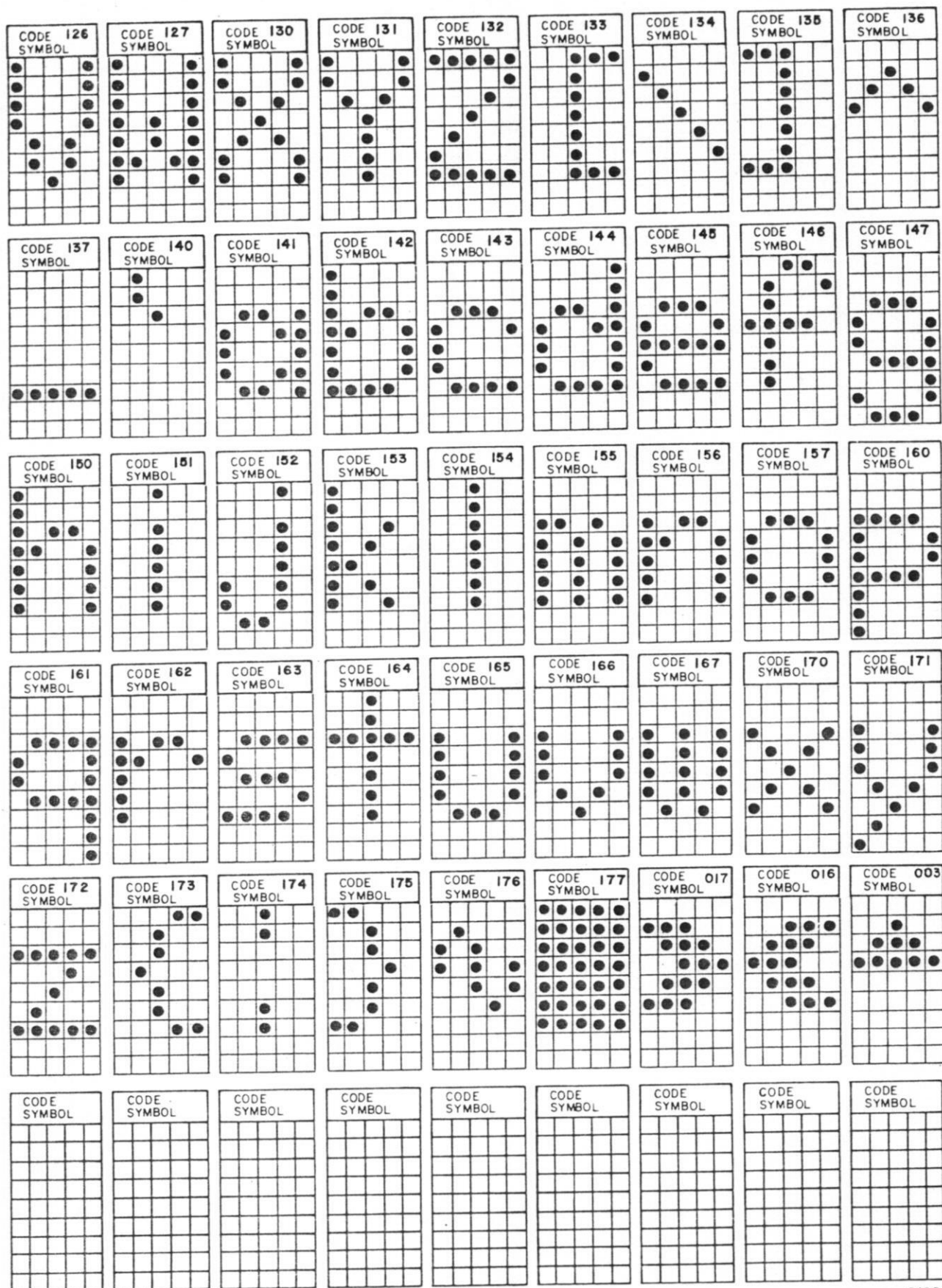
Figure 7-5 shows the first scan line for formation of the character H, using pin 13 of B1, Diagram 005, as the test point.

Figure 7-6 is a logic troubleshooting chart to provide a method of isolating a fault in the logic module.



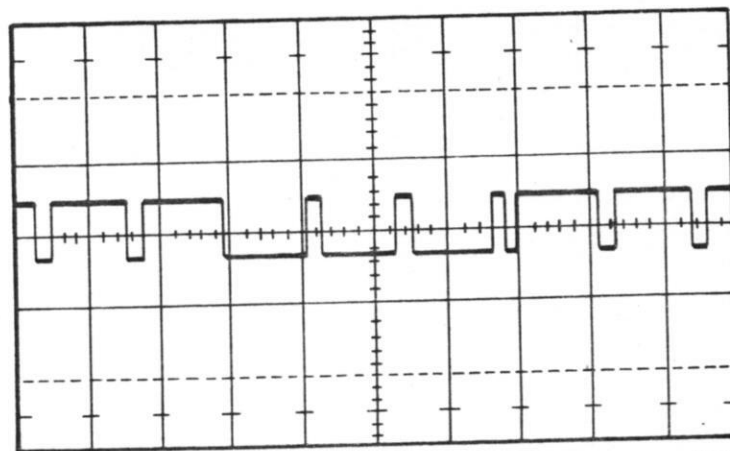
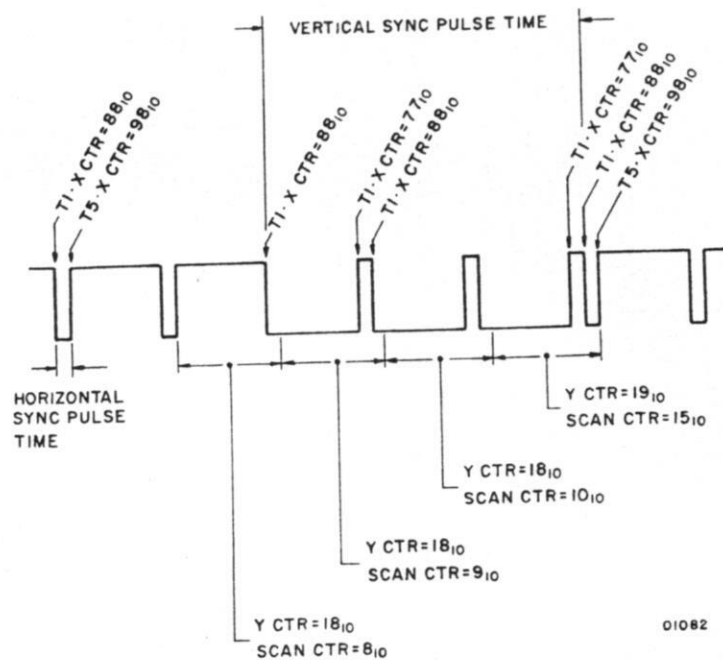
01093

Figure 7-1. Symbol Formations (Sheet 1)



01092

Figure 7-1. Symbol Formations (Sheet 2)

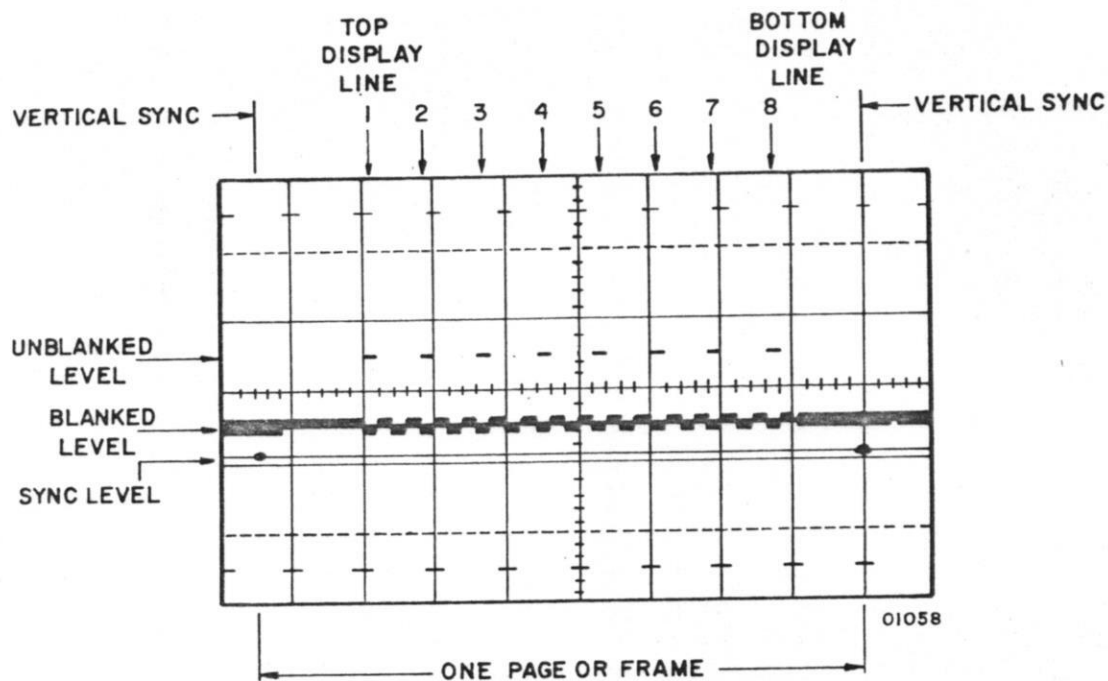


Waveform: Horizontal and Vertical Sync Pulses
 Test Pattern: No Display
 Test Point: Base of K1Q4 (Diagram 008)

Oscilloscope Control Settings

VOLTS/CM	0.1v	SLOPE	+
TIME/CM	0.05 ms	COUPLING	AF LF REJ
MAGNIFIER	10X	SOURCE	EXT.
MODE	TRIG.	TRIGGER INPUT	TRIGGER OUTPUT (jumper)
		SYNC INPUT	CHANNEL B to Y2 ⁴ (A9-6, Diagram 001)

Figure 7-2. Horizontal and Vertical Sync Pulses

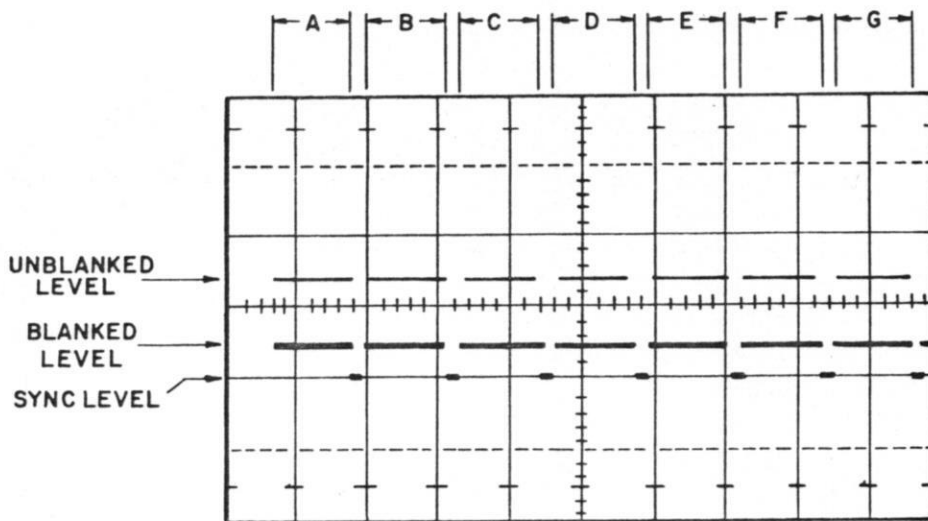


Waveform: Eight Display Lines of H's
 Test Pattern: Full Raster of H's
 Test Point: Base of K1Q4 (Diagram 008)

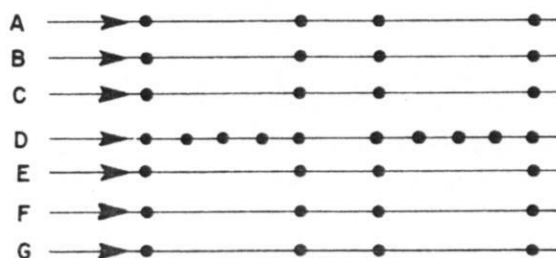
Oscilloscope Control Settings

VOLTS/CM	0.2v	SLOPE	+
TIME/CM	0.2 ms	COUPLING	AF LF REJ
MAGNIFIER	OFF	SOURCE	EXT.
MODE	TRIG.	TRIGGER INPUT	TRIGGER OUTPUT (jumper)
		SYNC INPUT	CHANNEL B to Y2 ⁴ (A9-6, Diagram 001)

Figure 7-3. Eight Display Lines of H's



01059

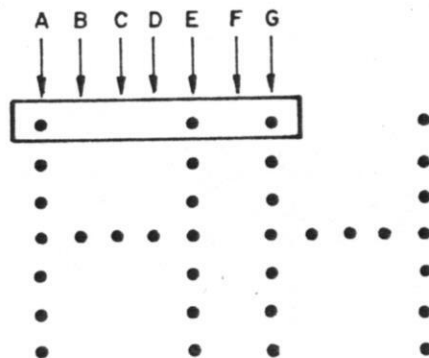
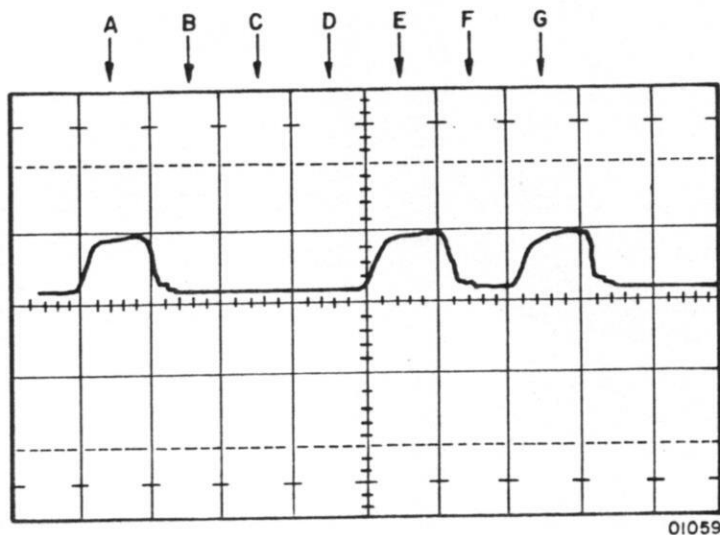


Waveform: Full Display Line of H's
 Test Pattern: Full Raster of H's
 Test Point: Base of K1Q4 (Diagram 008)

Oscilloscope Control Settings

VOLTS/CM	0.2v	SLOPE	+
TIME/CM	50.0 μ sec	COUPLING	AF LF REJ .
MAGNIFIER	OFF	SOURCE	EXT.
MODE	TRIG.	TRIGGER INPUT	TRIGGER OUTPUT (jumper)
		SYNC INPUT	CHANNEL B to Y2 ⁴ (A9-6, Diagram 001)

Figure 7-4. Full Display Line of H's

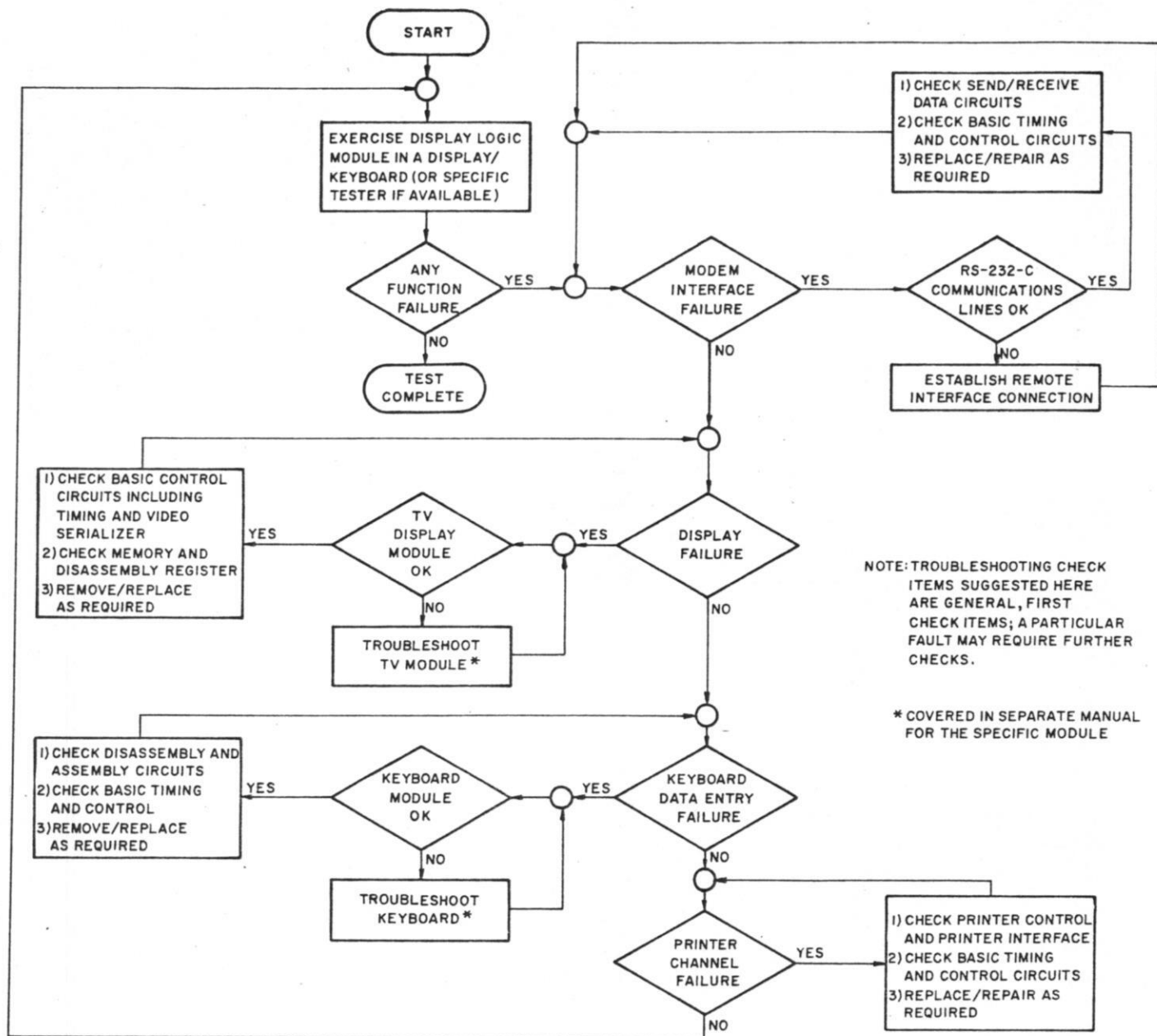


Waveform: First Scan Line of H's
 Test Pattern: Full Raster of H's
 Test Point: B1-1 (Diagram 005)

Oscilloscope Control Settings

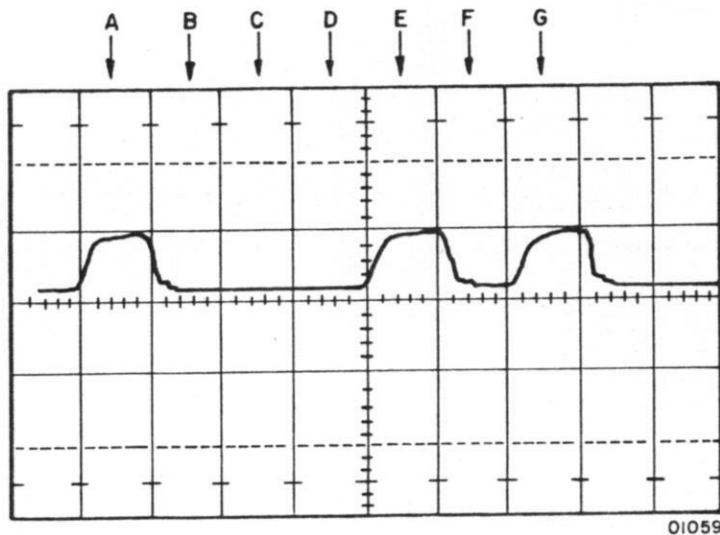
VOLTS/CM	0.5v	SLOPE	+
TIME/CM	0.1 μ sec	COUPLING	AF LF REJ
MAGNIFIER	OFF	SOURCE	EXT.
MODE	TRIG.	TRIGGER INPUT	TRIGGER OUTPUT (jumper)
		SYNC INPUT	CHANNEL B to same as Test Point

Figure 7-5. First Scan Line of H's

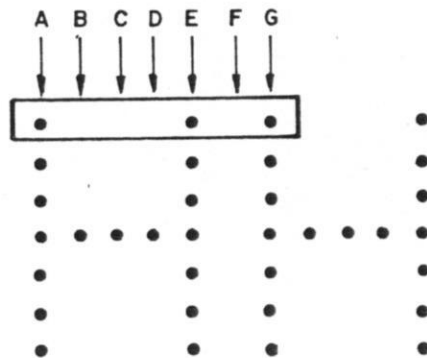


01084

Figure 7-6. Logic Troubleshooting Chart



01059

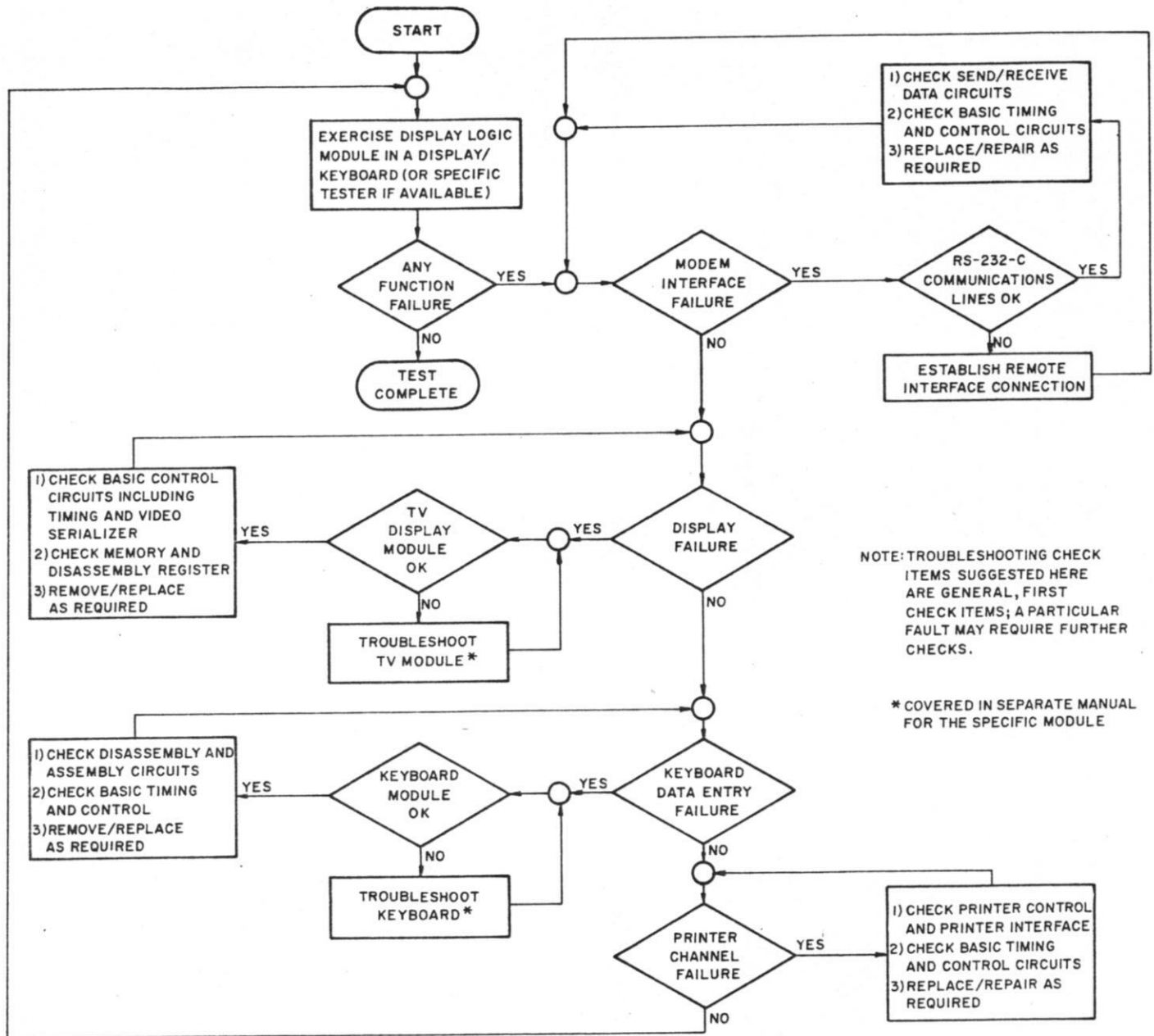


Waveform: First Scan Line of H's
 Test Pattern: Full Raster of H's
 Test Point: B1-1 (Diagram 005)

Oscilloscope Control Settings

VOLTS/CM	0.5v	SLOPE	+
TIME/CM	0.1 μ sec	COUPLING	AF LF REJ
MAGNIFIER	OFF	SOURCE	EXT.
MODE	TRIG.	TRIGGER INPUT	TRIGGER OUTPUT (jumper)
		SYNC INPUT	CHANNEL B to same as Test Point

Figure 7-5. First Scan Line of H's



01084

Figure 7-6. Logic Troubleshooting Chart

SECTION 8

PARTS DATA

This section contains the assembly information for the logic module down to the logic card level. Details of the components contained on a logic card are given in the IAT display logic module circuit cards described in the foreword.

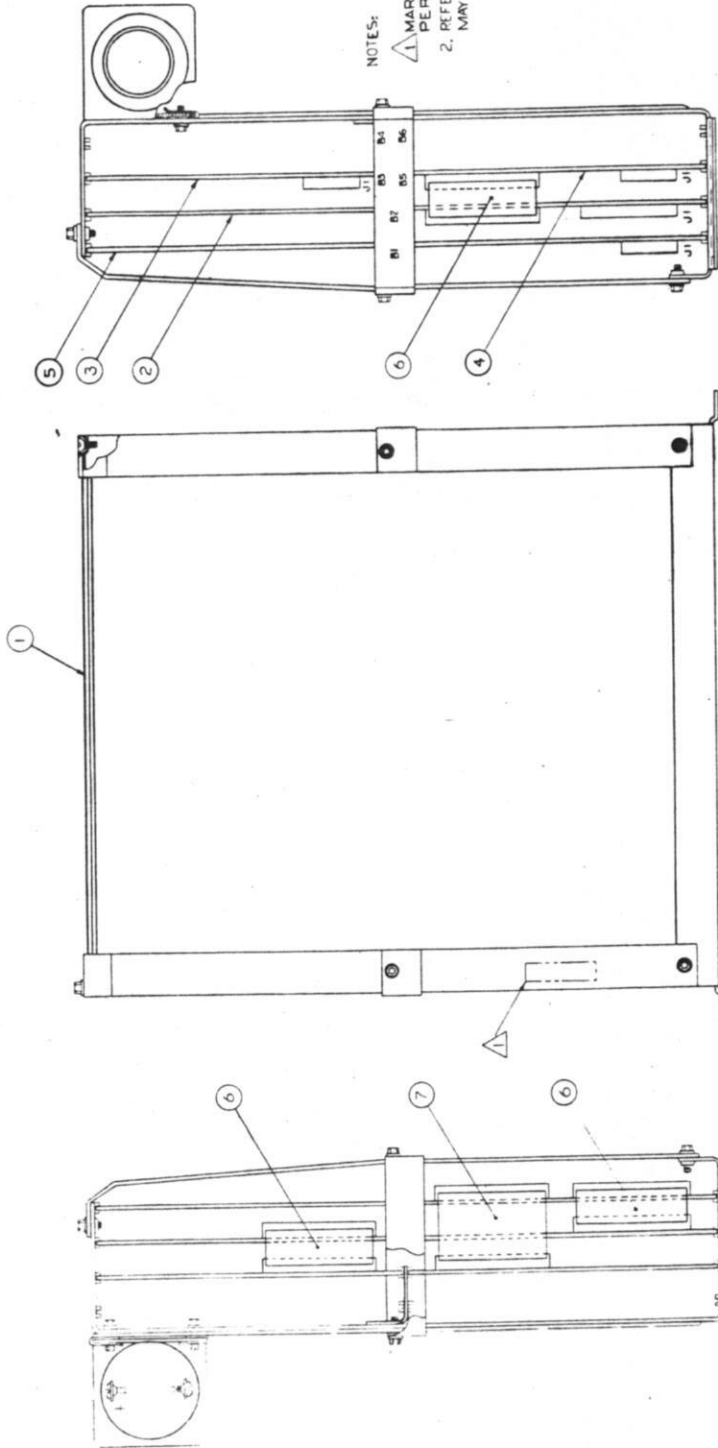
Table 8-1 explains the column headings for the parts lists contained in this section.

TABLE 8-1. EXPLANATION OF COLUMN HEADINGS OF ASSEMBLY PARTS LISTS

COLUMN HEADING	EXPLANATION
FIND NO.	Identifies an electrical or mechanical part on an assembly drawing. If more than one listing appears for a find number, refer to LI, WK IN, and WK OUT.
LI (Line Item)	Gives a chronological or historical record of the addition of a new part to a find number. For example, 01 indicates that the part was the first one used, and 02 indicates the second, etc. See also WK IN and WK OUT.
PART NUMBER	Gives the Control Data Corporation part identification. Use this number when ordering replacements.
CD (Check Digit)	Gives the information-control system a means of cross-checking the correctness of a part number.
QUANTITY	Lists the total number of a part required to complete an assembly. The vertical line near the center of the column acts as a decimal point. Numbers to the left of the line are whole numbers. Those to the right of the line are tenths, hundredths, and thousandths.
U/M (Unit of Measure)	Indicates how the information-control system counts or supplies a part.
PART DESCRIPTION	Describes the physical appearance, type, or name of a part.
MC (Material Control Code)	Supplies additional descriptive data to the information-control system.
YLD (Yield)	A 2-digit numeric number that indicates the usable portion of any quantity of parts expressed as a percentage.
ECO NO. IN	Engineering Change Order that adds a new part to an assembly. See also WK IN.
ECO NO. OUT	Engineering Change Order that deletes a part from an assembly. See also WK OUT.
S/N (Serial Number)	Used to specify an ECO's effectivity by serial number.
WK IN (Week In)	Lists the date when manufacturing begins using a new part and when it is available for parts replacement. For example, 7222 means a part is available as of the 22nd week of 1972.
WK OUT (Week Out)	Lists the date when manufacturing no longer uses a part in building an assembly. See also WK IN. Do not order a part after its week-out date.

0643

REVISION RECORD		REV	ECO	DESCRIPTION	DATE	BY
1	01	01	01	01	01	01
2	02	02	02	02	02	02
3	03	03	03	03	03	03
4	04	04	04	04	04	04
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NOTES:
 1. MARK ASSY 62163600 REV 1 IN AREA SHOWN PER CDC SPEC 1012150B, J12 HIGH, COLOR BLACK.
 2. REFERENCE DESIGNATIONS ARE REFERENCE ONLY AND MAY NOT APPEAR ON THE PART.

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PR

06/26/73	1
PROCESSING DATE	PAGE NUMBER



ASSEMBLY PARTS LIST

SPARE CODE
S - SPARE PARTS
N - NON SPARE PARTS

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001	61206800	1	00	PC LOG CHASS ASSY	IN					1	S12A		
002	62149300	1	00	PC CARD ASSY 1FDE	IN					1	A12A		
003	90137100	1	00	PC CARD ASSY 0JMD FOR T 128.00	IN					1	A12A		
004	90252400	1	00	PC CARD ASSY 2ASD	IN					1	A12A		
005	62081800	1	00	PC PC ASSY 1CGE	IN					1	A12A		
006	61207003	3	00	PC CBL ASSY S10 JUMPER	IN					1	S12A		
007	61207004	1	00	PC CBL ASSY S10 JUMPER	IN					1	S12A		
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PROJECT ENGINEER

AA 210

REV. 2-78

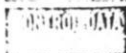
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001	01	71273500	0		1		PC CHASSIS-LOGIC LCOM	P			00000000			7101				
001	02	62015400	5		1		PC CHASSIS-LOGIC	P		00000000				7101				
002	01	71273400	3		1		PC STRAP-RETAINING	P			00000000			7101				
002	02	62015000	3		2		PC STRAP RETAINER	P		00000000	DT00312			7101 7148				
002	03	62131900	3		1		PC COVER LOGIC CHASSIS	P		DT00312				7148				
003	01	71274600	7		1		PC RETAINER CARD	P			00000000			7101				
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004	02	62027800	2		1		PC DECAL ADHESIVE BACKED	P		00000000				7146				
005	01	61207000	3		3		PC SIGNAL JUMPER CABLE ASSY	A			00000000			7101				
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006	01	90136700	3		1		PC CARD ASSEMBLY OJFD	A			00000000			7101				
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007	01	90136500	7		1		PC CARD ASSEMBLY OJED	A			00000000			7101				
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009	01	51003800	3		1		PC SOUND ALARM INDICATOR, ELECTR	P			00000000			7101				
009	02	00838200	4		2		PC NUT (U) TYPE 6/32	B		00000000				7146				
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011	01	10125605	5		4		PC WASHER FLT NO.6 STEEL	B			00000000			7101				
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0028 TOTAL LINES																		

61207000	C	CLA	A	CBL ASSY SIG JUMPER	CD				
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PR

07/11/73	1
PROCESSING DATE	PAGE NUMBER



ASSEMBLY PARTS LIST

SPARE CODE
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N - NON SPARE PARTS

FIND NUMBER	SW	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY	PN	NC	W
001		51768700	76	00	PC CONTACT PIN CRIMP FLAT CBL	IN						P11A		
002		51768802	2	00	PC CONN PIN HOUSING	IN						P11A		
003		95034101	23	FT	FLAT CABLE	IN						P11C		

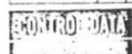
AA 270 PROJECT ENGINEER

REV. 2-78

61207000	C	CLA	A	CBL ASSY SIG JUMPER	CD				
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PR

06/21/73	1
PROCESSING DATE	PAGE NUMBER



ASSEMBLY PARTS LIST

SPARE CODE
S - SPARE PARTS
N - NON SPARE PARTS

FIND NUMBER	SW	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY	PN	NC	W
001		51768700	76	00	PC CONTACT PIN CRIMP FLAT CBL	IN				1	P11A			
002		51768802	2	00	PC CONN PIN HOUSING	IN				1	P11A			
003		95034101	33	FT	FLAT CABLE	IN				1	P11C			

AA 270 PROJECT ENGINEER

REV. 2-78

STAPLE

STAPLE

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FOLD

FIRST CLASS
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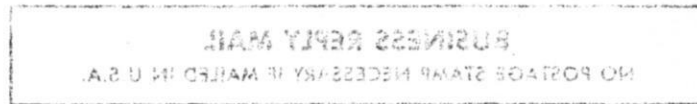
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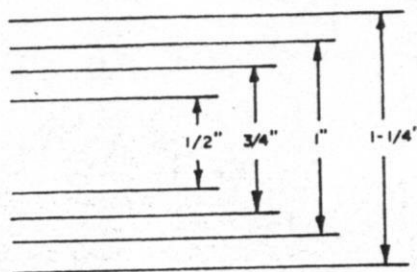
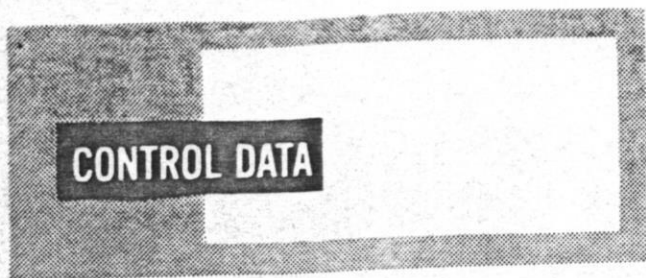
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